P0 Transverse feedback development

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Contributors

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Acknowledgements

Leonard Morrison, Suk Kim, Yong-chul Chae, Chuck Gold, Bob Laird, Pat Dombrowski, Louis Emery, Frank Lenkszus, Randy Zabel, Glenn Decker, Hang Bui, Bob Lill, M. Borland, T. Nakamura, J. Fox, Louis Emery.

Outline

- Project history
- Recent test results
- Some background on feedback systems
- System description
- Further upgrade plan

System objective

- APS storage ring beam instabilities are mainly controlled with chromaticity adjustment:
  - Chromaticities of 6 to 7 are necessary for 24 singlet fill
  - and 11 to 12 for hybrids fill due to high single-bunch charge (16mA) in the leading bunch.
  - Some sextupole are at maximum current even after the pole tips are shimmed to increase flux.
- High chromaticity has some side effects:
  - reduces beam dynamic aperture and shortens beam lifetime.
  - Also makes the injection close-bump hard to match.
  -
- New development of APS upgrade lattice requires to use feedback system to stabilize beam with reduced chromaticity.

System objective (cont.)

- Reduce chromaticity while keep beam stable.
- Increase beam lifetime.
- Increase single bunch beam current accumulation limit.
- As an additional tool for development of high current or low emittance configurations in the future.

Project history and status

- 2007 and before: Proposal, design, component test.
- 2008: FPGA development and system integration. Started closed-loop test.
- 2009: major improvement to overcome insufficient horizontal drive.
  - Two new 500-Watt amplifiers.
  - A new longer horizontal kicker stripline.
  - New location in S35 for the horizontal stripline which has high betax.
  - Remote DAC through fiber link to transmit data stream from S2 to S35 with a rate of 2.36 GBS.
- 2010: completed 24-singlet and hybrids-fill test with reduced chromaticity of -2.0 in each plane.
- The system has been evaluated during user operation and will be used for user operations starting coming runs.

Ring parameters

Beam energy (E_0): 7 GeV.

Beta function at pickup (β_x /β_y): 6.28/24.34 m.

Beta function at kicker (β_x /β_y): 20.23/24.91 m (different locations).

Betatron tunes (ν_x/ν_y): 36.17/19.3.

Synchrotron Damping time (τ_x,τ_y): 9.6 /9.6 ms.

Harmonic number(h) 1296.

Bucket spacing: 2.84 ns.

Revolution frequency(f_0): 271 KHz.

Source size (σ_x,σ_y): 270(120)/11 μm.

System parameters

Required pickup resolution (μm): 10/2
Required noise level (μm): 5/2
Dynamic range (μm): 1000/500
stripline kick strength(μRad): 0.78 / 0.26
Actual A/D bits : 14/14
Actual DAC bits: 14/14
Sample rate(MHz): 117 (352*)
Damping time: 0.5 ms / 0.05 ms**

* with FPGA upgrade
** Measured.

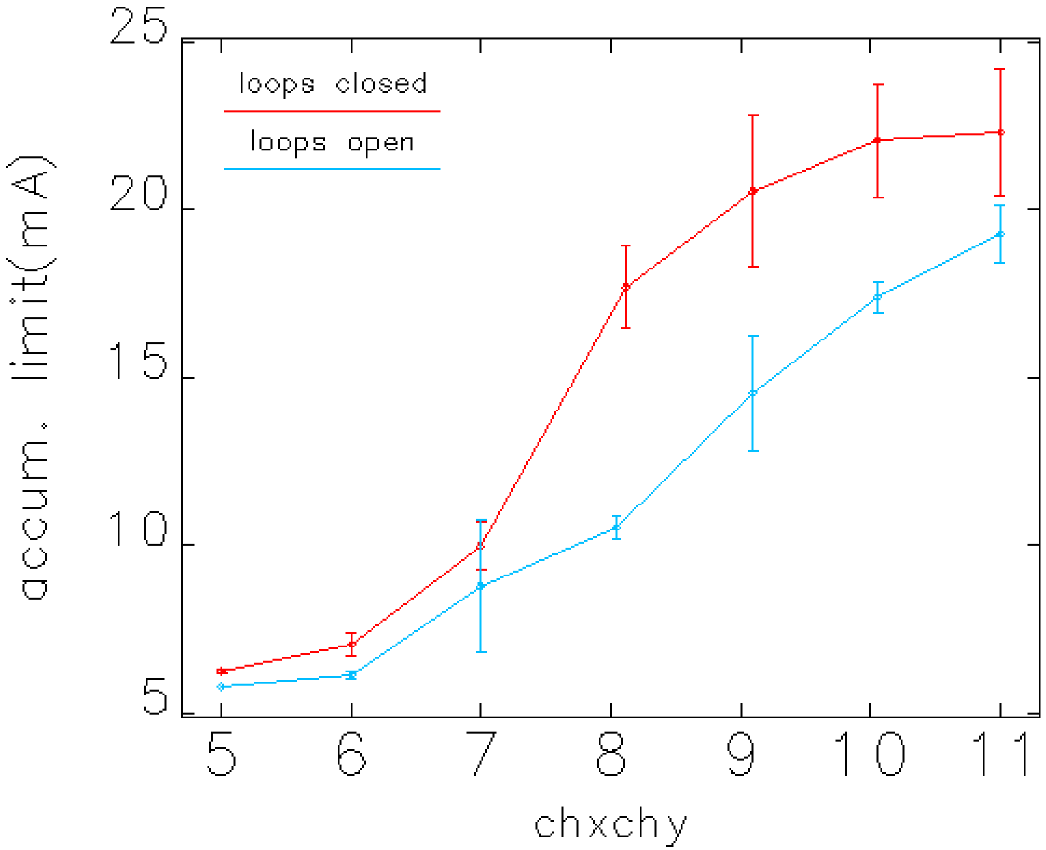
Recent test results

Table1: Beam parameters of 24-singlet fill with and without feedback.

	Loops open	Loops closed
chx/chy	7/6	3/2
x-emitt.(nm)	2.45	2.5
y-emitt.(nm)	0.054	0.06
coupling(%)	2.2	2.22
xRMS-30Hz (um)	2.73	2.45
xRMS-full BW(um)	8.72	6.05
yRMS-30Hz (um)	1.24	0.75
YRMS-full BM(um)	2.96	3.17
Beam life(min.)	443	878

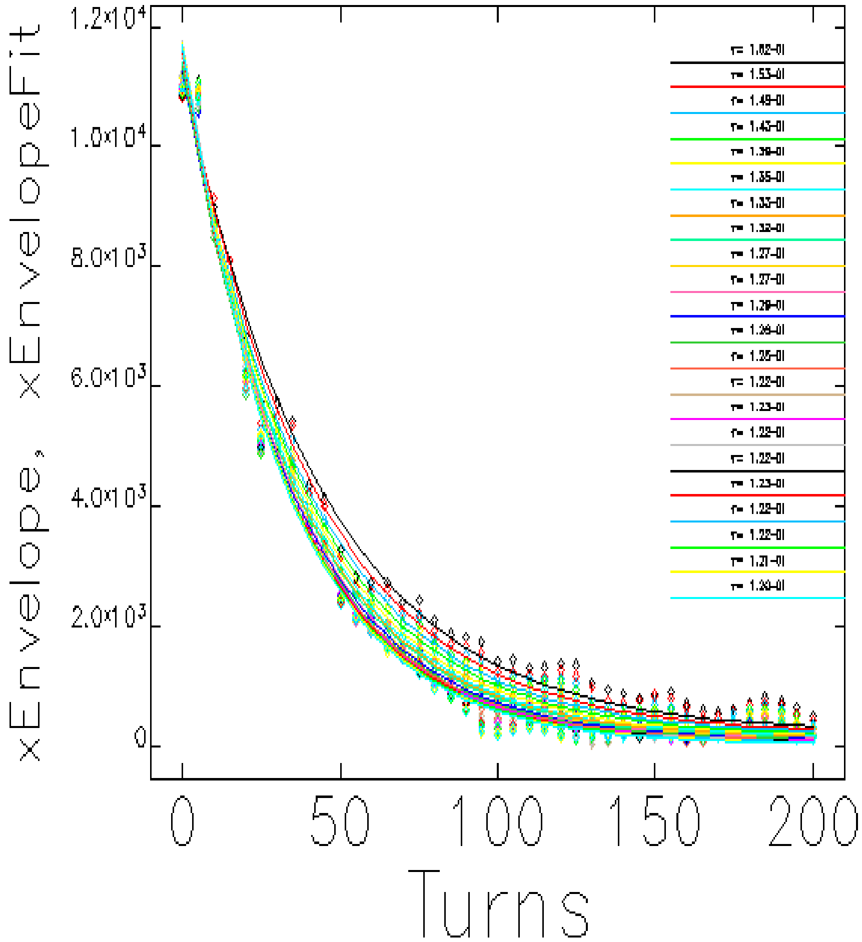
Single-bunch accumulation limits

- Usable configuration for hybrids pattern
  - Chx=8.34
  - Chy=8.76
  - Accumulation limits > 20 mA
- Without feedback:
  - Chx =10
  - Chy =11
- Data taken before the vertical steering effect was discovered and corrected[1].

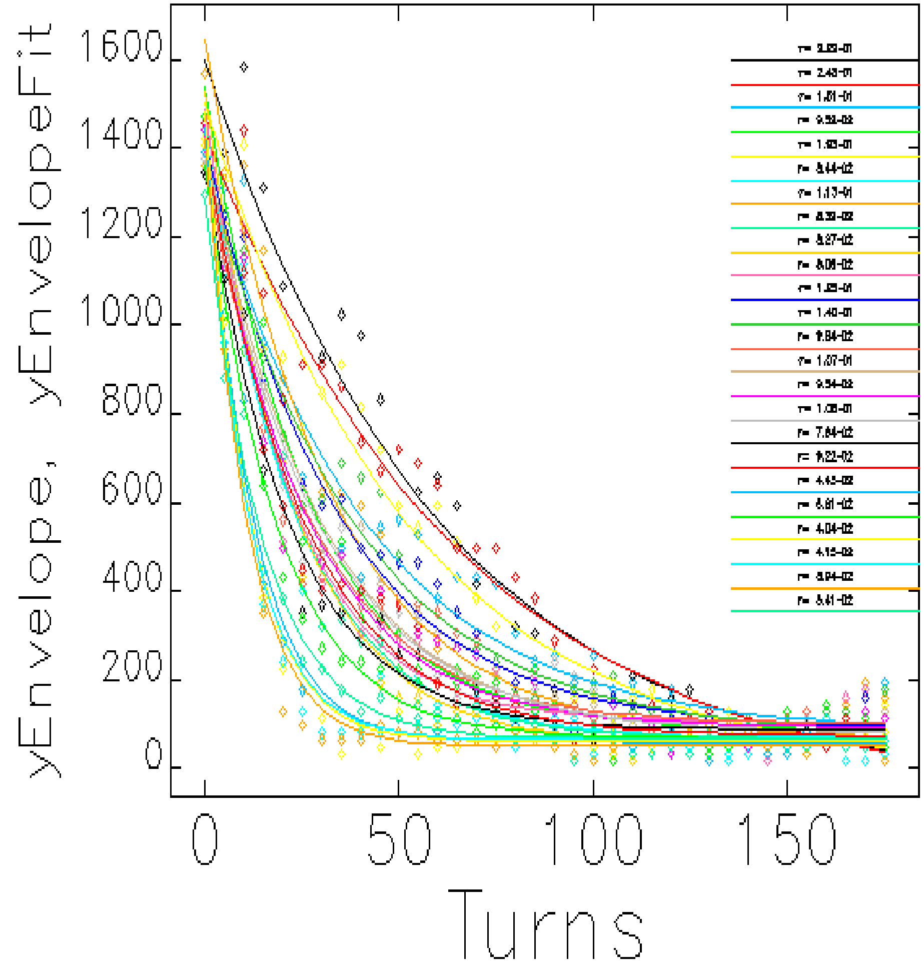


[1] Vadim Sajaev and Louis Emery

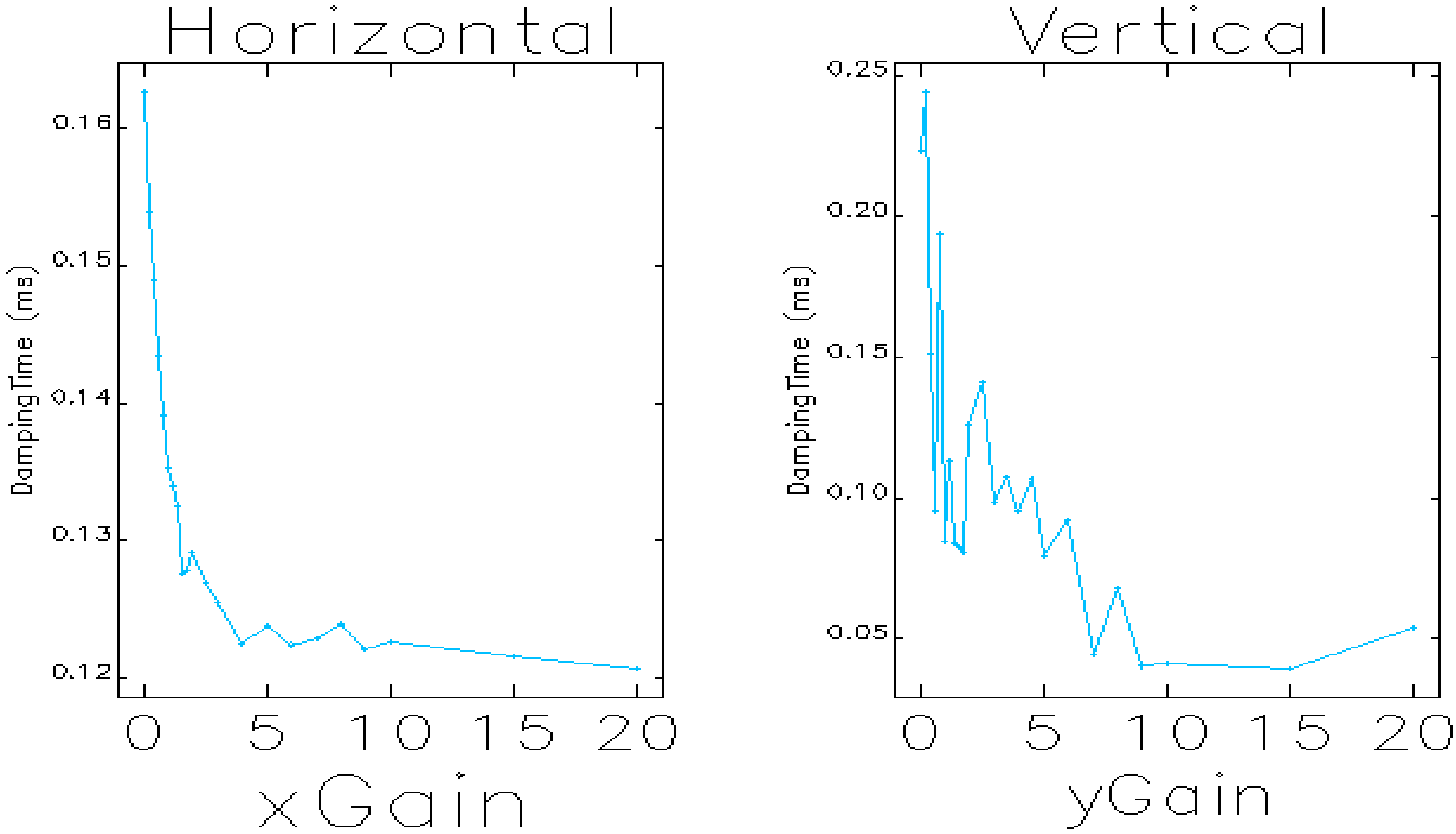
Damping measurement with kicking method



Horizontal plane



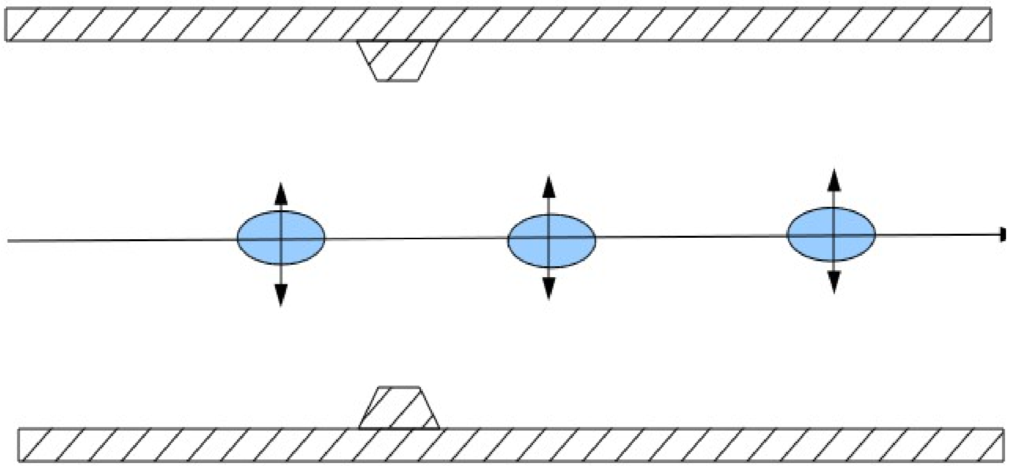
Vertical plane



Horizontal
Damping Time (ms)
0.16
0.15
0.14
0.13
0.12
0
5
10
15
20
xGain
Vertical
Damping Time (ms)
0.25
0.20
0.15
0.10
0.05
0
5
10
15
20
yGain

A simple physics model of transverse feedback system

- Bunches move along the vacuum chamber. They also go through betatron oscillations.
- Bunch interacts with vacuum chamber impedance and produce both longitudinal and transverse fields.
- These field interacts with the bunches and causes feedback to bunches and instability.
- A feedback system detects the beam motion and produces a damp term that is proportional to X'.



$$X'' + \omega_x^2 X + (G + D) X' = 0$$

Mode-based and bunch-by-bunch feedback

- Beam instabilities can be separated in modes, characterized by its mode frequency and phase pattern.
- Mode-based feedback system detects oscillation of each mode and damps it with one frequency channel.
- It is also called frequency-domain method.
- It is impractical if there are too many unstable coupled bunch modes.
- Bunch-by-bunch feedback works in time domain.
- It detects oscillation of each bunch and damps each bunch with common feedback channel. Bunches are separated in time slots.
- The physics base is that if the motion of all bunches are damped individually all the modes will also be damped.

Digital and analog feedback

- Analog feedback systems use stripline and BPM and RF filter, attenuator, delay line, and amplifiers to detect beam motion and process feedback output signal.
- Digital feedback systems first sample pickup signal into digital data and process data digitally, and then convert output data to analog waveform to drive beam.

Spectrum of bunched electron beam

Without transverse oscillation:

$$i(t)=i_0\sum_{-\infty}^{+\infty}\delta(t-nT_0)$$

$$I(\omega)=I_0\sum_{n=-\infty}^{+\infty}\delta(\omega-2\pi n f_0)$$

With transverse oscillation:

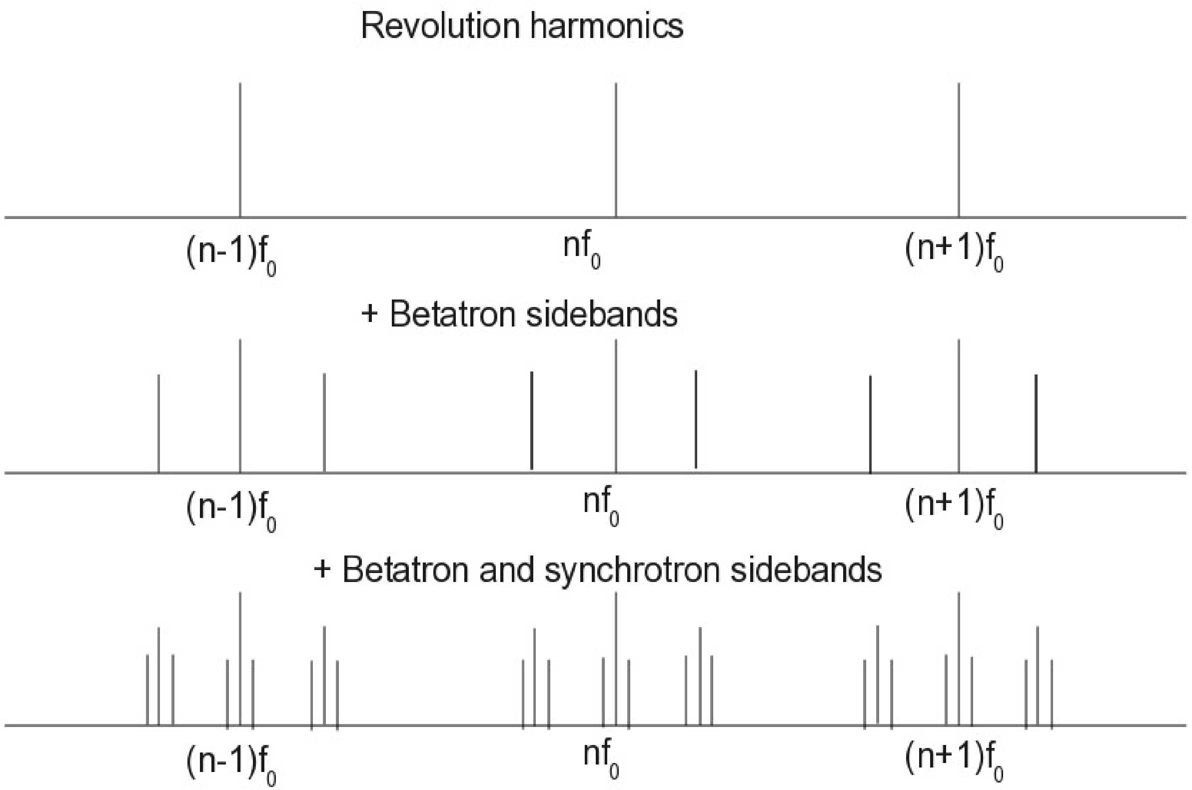
$$i(t)=i_0\sum_{-\infty}^{+\infty}\delta(t-nT_0)e^{-j\omega_x t}$$

$$I(\omega)=I_0\sum_{n=-\infty}^{+\infty}\delta(\omega-2\pi n f_0-\omega_x)$$

With longitudinal time oscillation:

$$i(t)=i_0\sum_{-\infty}^{+\infty}\delta(t-nT_0-\tau\cos(\omega_s t))$$

$$I(\omega)=I_0\sum_{m=-\infty}^{+\infty}(-j)^k J_m(\omega\tau)\sum_{-\infty}^{+\infty}\delta(\omega+m\omega_s-2\pi f_0)$$



FIR generation

- The FIR filters are at the core of a feedback system.
- There are two basic methods in FIR generation:
- Frequency domain method:
  - specify desired frequency character.
  - derive the filter coefficients with DFT.
- Time domain least square fitting (TDLSF) method[1]:
  - Specify time domain character.
  - Derive filter coefficients by least square fitting.
- We implemented the TDLSF method.

[1] T. Nakamura

$$\begin{bmatrix} x_{n-k} \\ x'_{n-k} \end{bmatrix} = M^{-k} \begin{bmatrix} x_n \\ x'_n \end{bmatrix}$$

$$M^{-k} = \begin{bmatrix} \cos(2\pi\nu k) + \alpha \sin(2\pi\nu k) & \beta \sin(2\pi\nu k) \\ -\gamma \sin(2\pi\nu k) & \cos(2\pi\nu k) - \alpha \sin(2\pi\nu k) \end{bmatrix}$$

$$\chi^2 = \sum_{k=0}^{k=M-1} [x(n-k) - C_k x_n - \alpha S_k x_n - \beta S_k x'_n]^2$$

$$C_k = \cos(2\pi\nu k) \qquad S_k = \sin(2\pi\nu k)$$

$$x'_n = \sum_{k=0}^{k=M-1} A_k x(n-k) \qquad x_n = \sum_{k=0}^{k=M-1} B_k x(n-k)$$

Ideal phase response

Two sampled sequences:

x(n) beam position at pick-up

x'(n) beamslpe at kicker

The phase difference between the two sequences can be expressed analytically as:

$$\Delta\theta = \frac{\pi}{2} + \tan^{-1}\alpha_k + \Delta\psi$$

α_k – alpha function at kicker

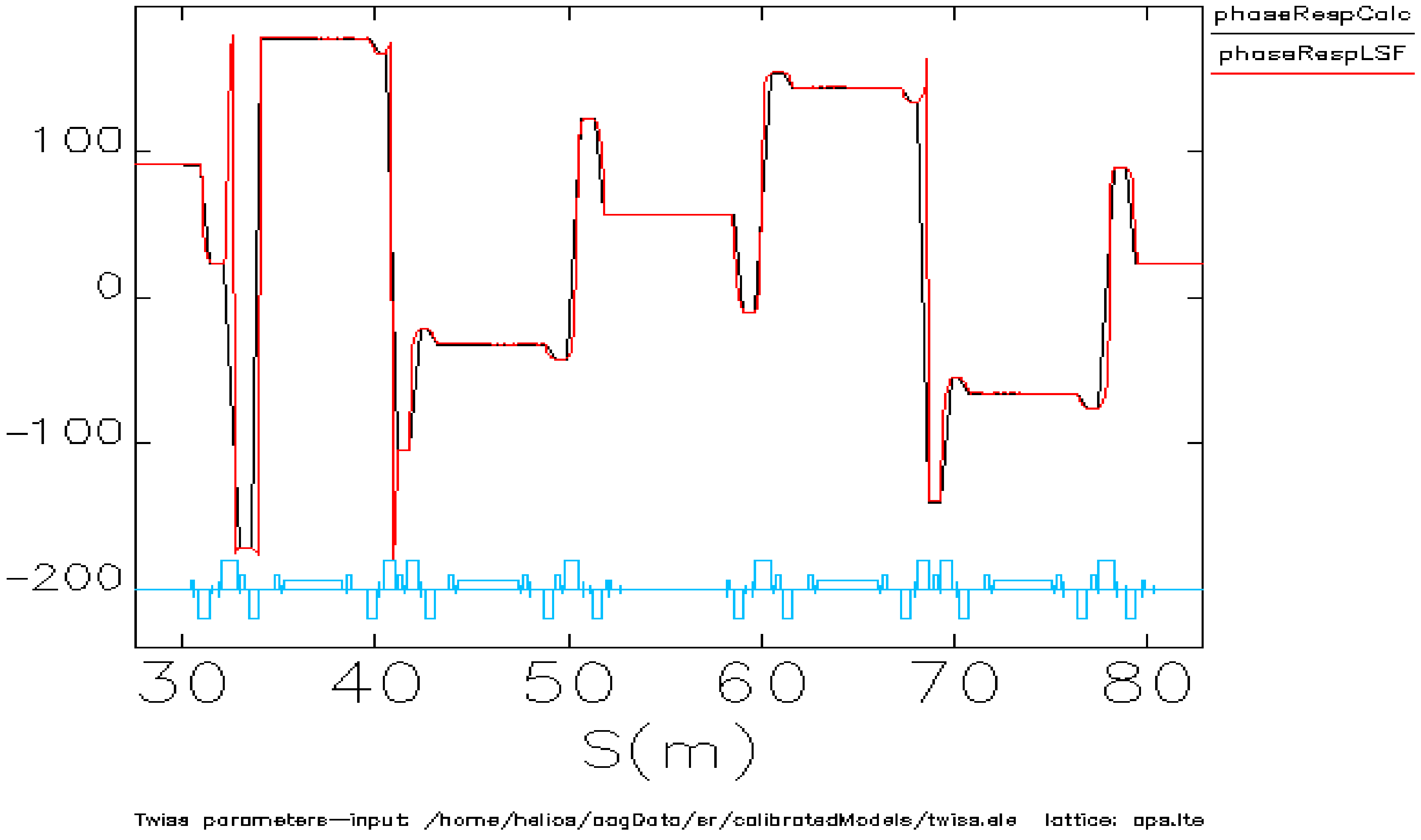
Ψ – betatron phase difference between kicker and pick-up

A simplest case: α_k=0 and Δψ=0:

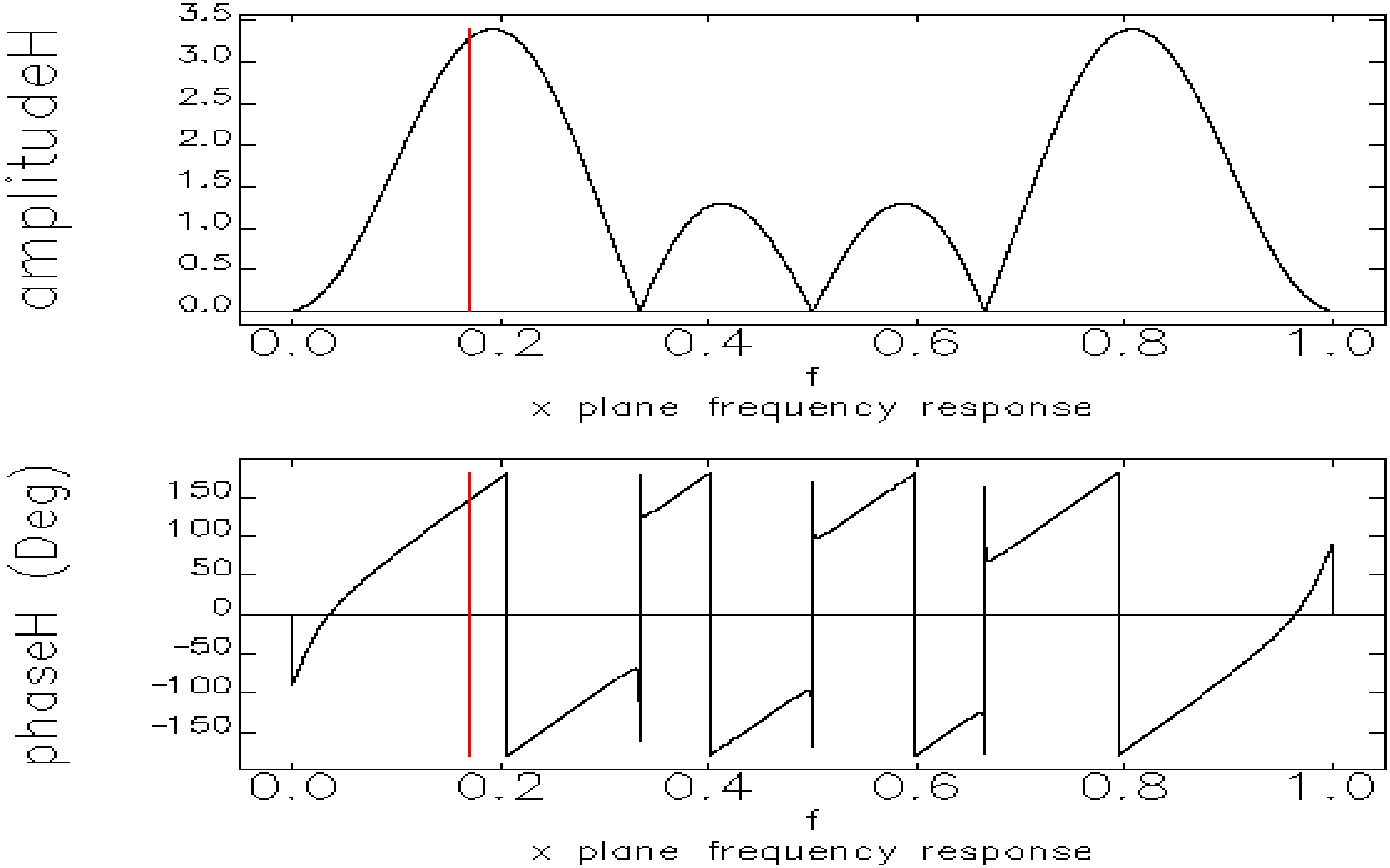
$$\Delta\theta = \frac{\pi}{2}$$

It is verified numerically that when turns number is larger than 3 the filter generated with TDLSF produces an exact phase response.

This validates that TDLSF method and frequency domain method are equivalent.



Ideal phase response (black) calculated from APS model lattice parameters and phase response of a 6-tap filter generated with TDLSF method (red).



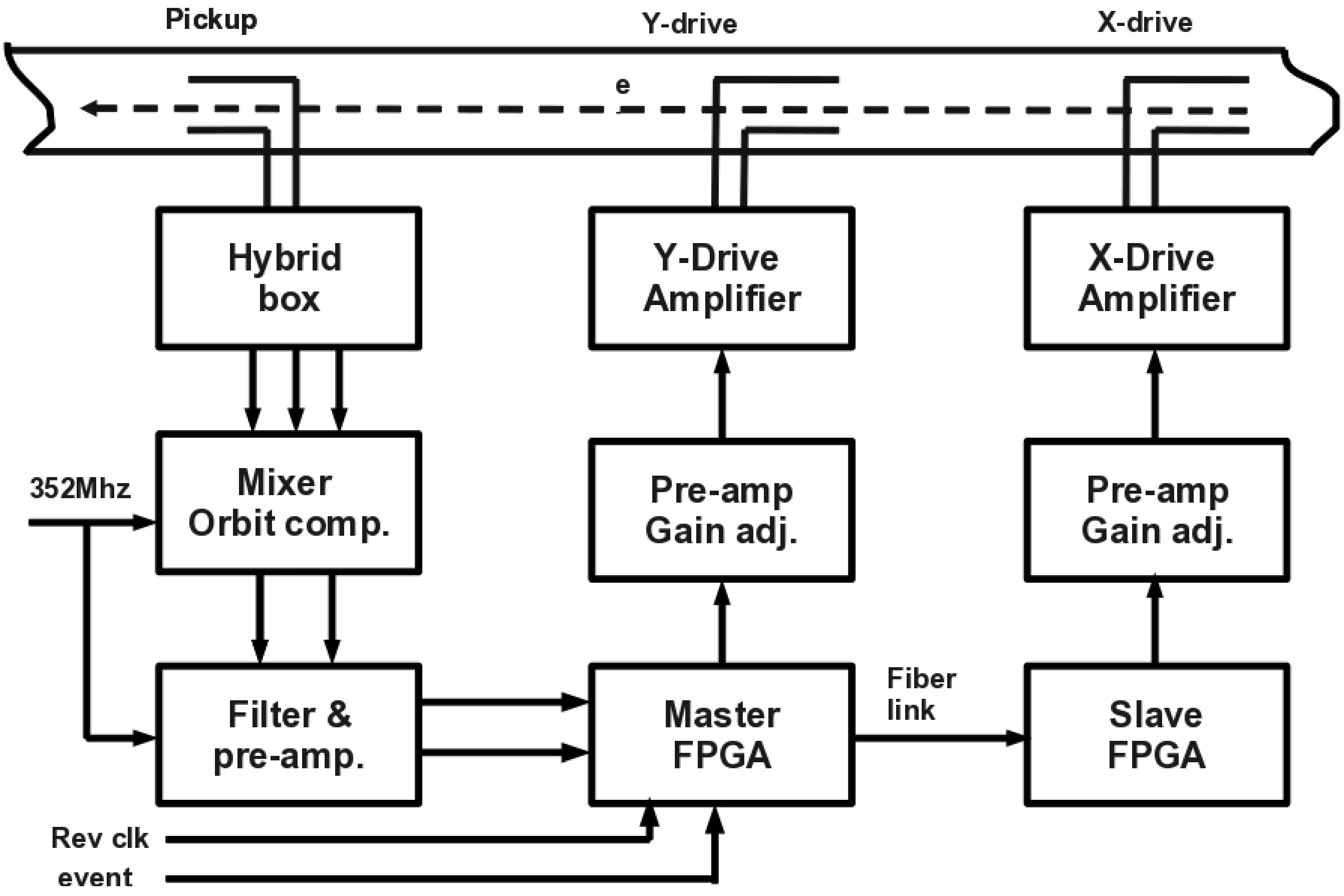
Frequency response 6-tap filter

Advantages and limitations of TDLSF

- Advantages:
  - Directly generates FIR from lattice file.
  - Close to ideal phase response.
  - Applies to locations where alpha is non-zero for pick-up and driver.

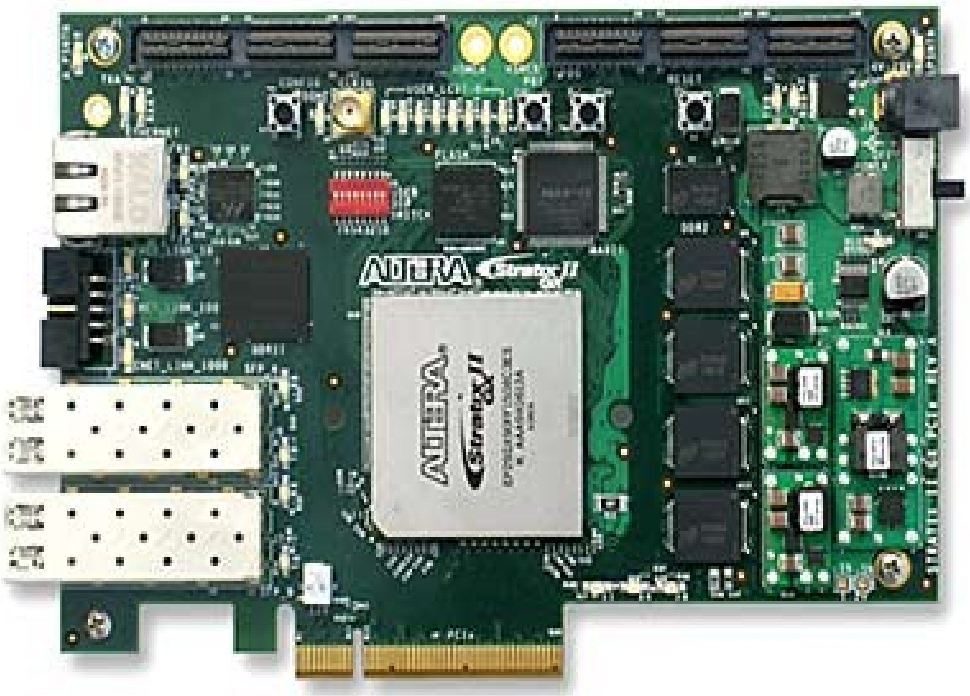
- Limitations:
  - The linear matrix does not include damping effect of the feedback. It is only applicable if the effect is relatively weak.
  - The method applies linear lattice model to centroid motion, which does not include tune shift produced by impedance or non linearity of lattice.

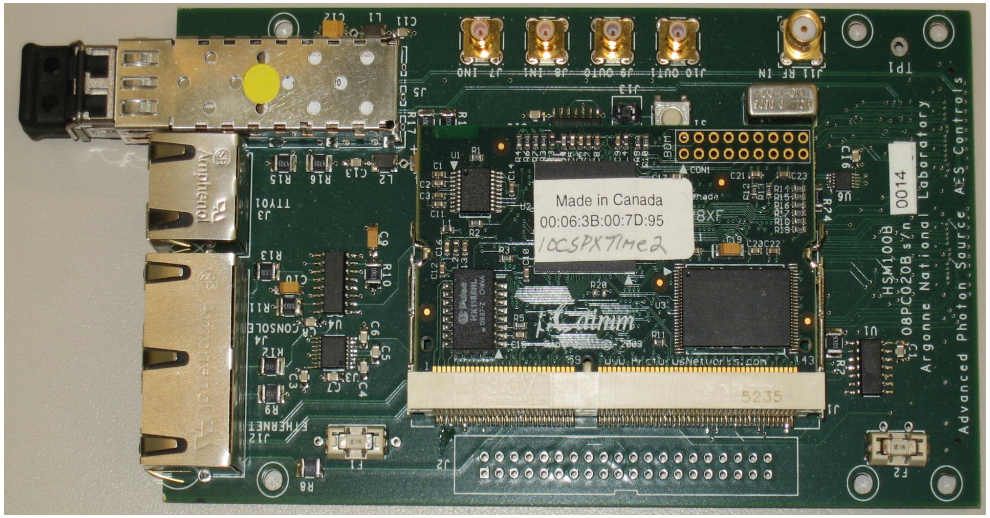
System Diagram



FPGA hardware config.

- Altera stratixII-GX DSP development kit
- PCI Express Fast Lane for digital communication between the master and slave processors.
- SLS HSMC data conversion card:
  - 2x 14-bit A/D, max. sample rate 150 MSPS
  - 2x 14-bit DAC max. sample rate 250 MSPS
- Coldfire card as EPICS processor
- Home made HSMC daughter card for:
  - Clock/timing input
  - Fibre interface for event inputs
  - Ethernet connection
- An upgraded spare is under development:
  - StratixIV-GX DSP kit.
  - PCIE fiber interface for up to 8 GBS digital synchronous communication.
  - A home design data conversion board with 2x 14-bit and 2x 14-bit DAC with sample rate 400 MSPS.


ALTERA
Stratix II GX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ALTERA

Firmware features

- Up to 32-tap FIR filters.
- Filter coefficients are loaded on the fly.
- 2 channel waveforms for input data.
- 2 channel output data.
- Programmable output control pattern for output manipulation and diagnostics.
- Adjustable DAC delay in steps of clocks.
- Integrated Event Timing for synchronization to external event such as top-up injection.
- Built-in EPICS interface .

Sample control

+D	Normal
-D	Negate
CL	Copy last
NL	Negate last
Z	Zero
+V	Fixed positive
-V	Fixed negative

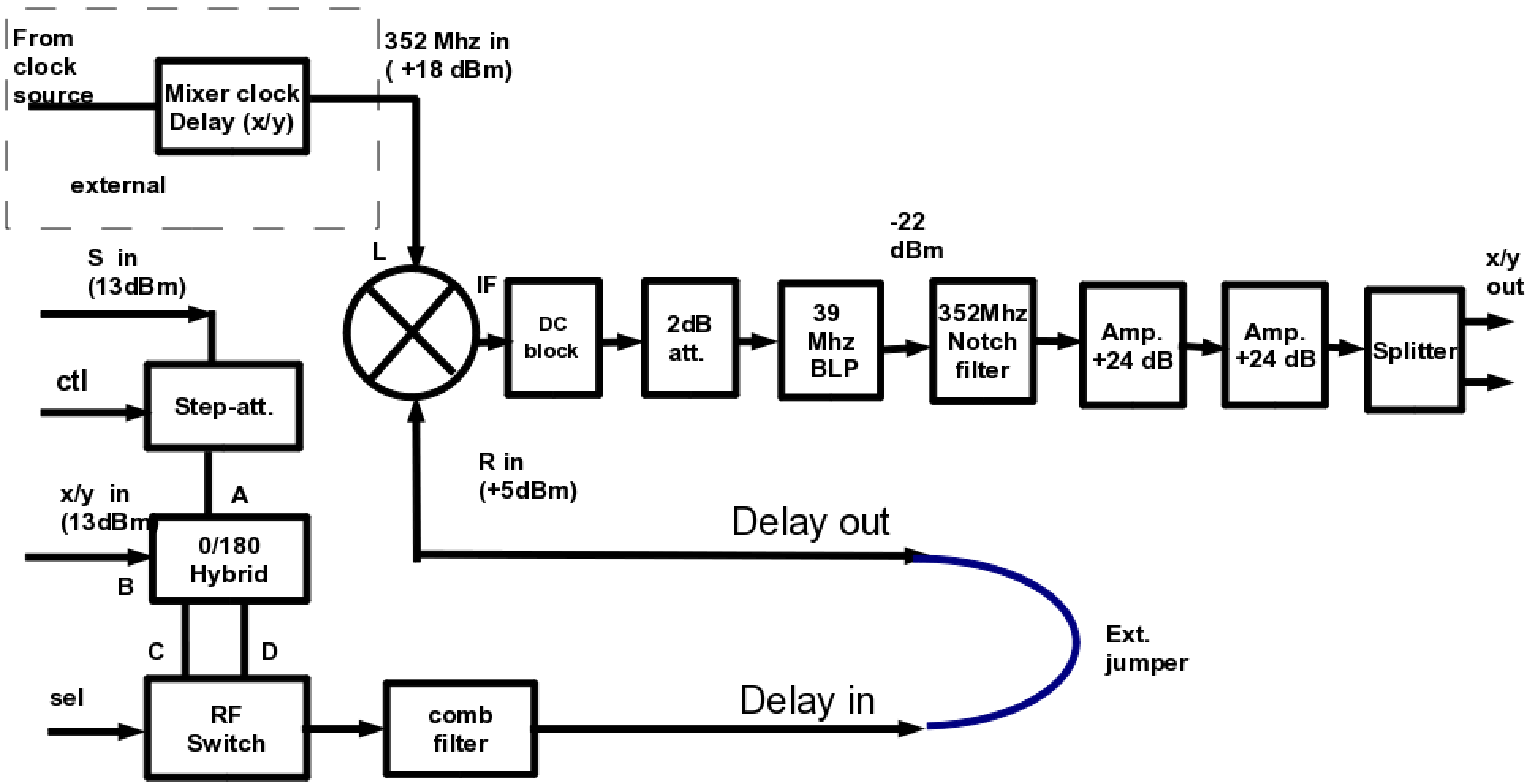
Drive system

- Amplifier:
  - 4 x 150-W, 10 Khz to 220 Mhz for vertical drive (diagonal 4 blades).
  - 2 x 500-W, 10 Khz to 250 Mhz for horizontal drive.
- Striplines:
  - Sector 4 for vertical drive:
    - Four-blade geometry.
    - Length: 16.7 cm
    - Measured kick: 0.26 µRad
  - Sector 35 horizontal drive:
    - Two blades geometry.
    - Length: 34 cm
    - Measured kick: 0.78 µRad

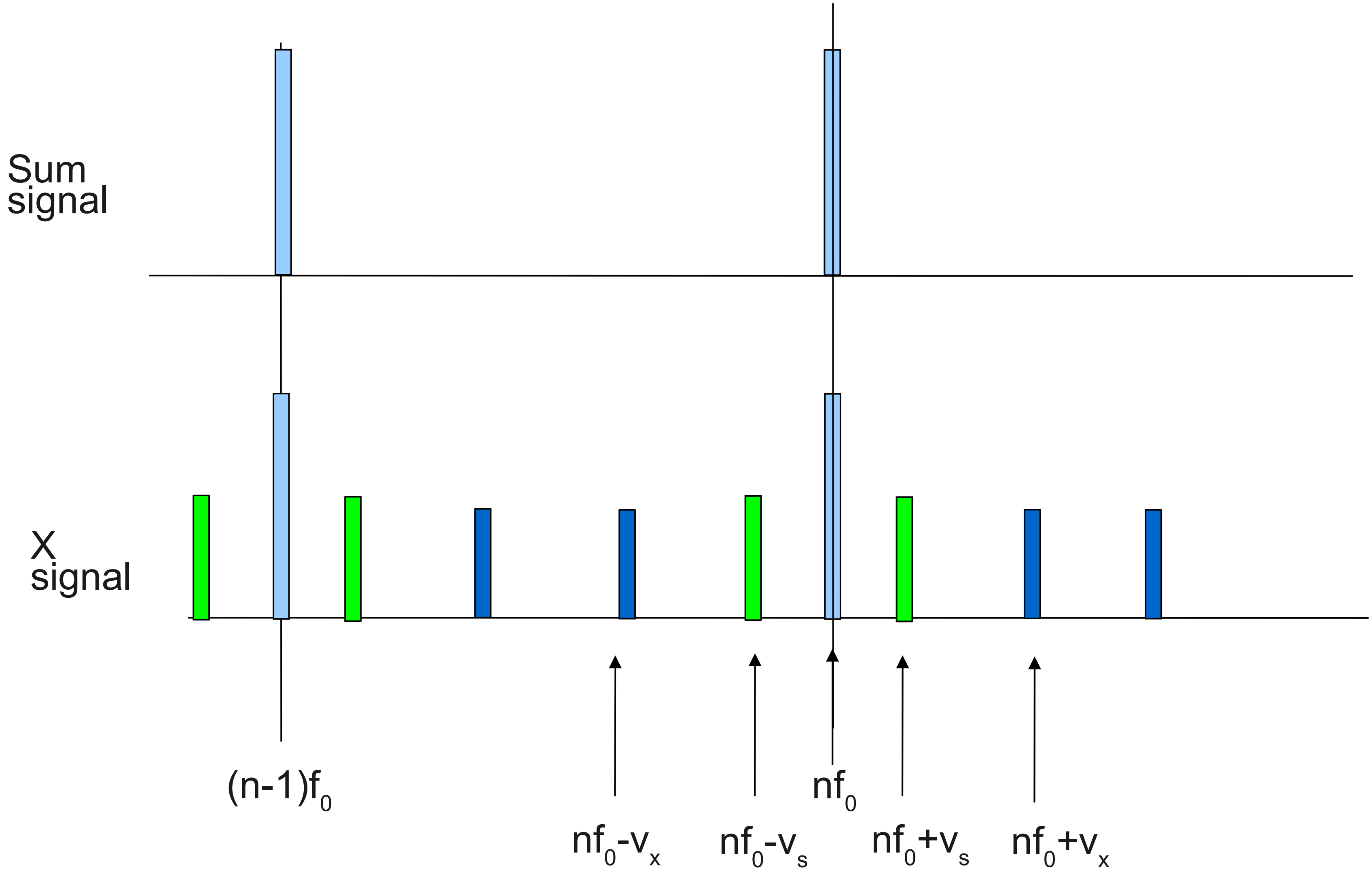
Front-end electronics

- Mixer/filter down converter.
- High level mixer (ZFY-2, 23 dB, 0.1 to 1000 MHz).
- 352 MHz LO input.
- Programmable delay for timing adjustment of LO input relative to beam signal
- Orbit component compensation circuit.
- Comb filter on stripline input signal.
- Bessel type LP filter on IF output.
- Low noise amplifiers.

Mixer /filter configuration



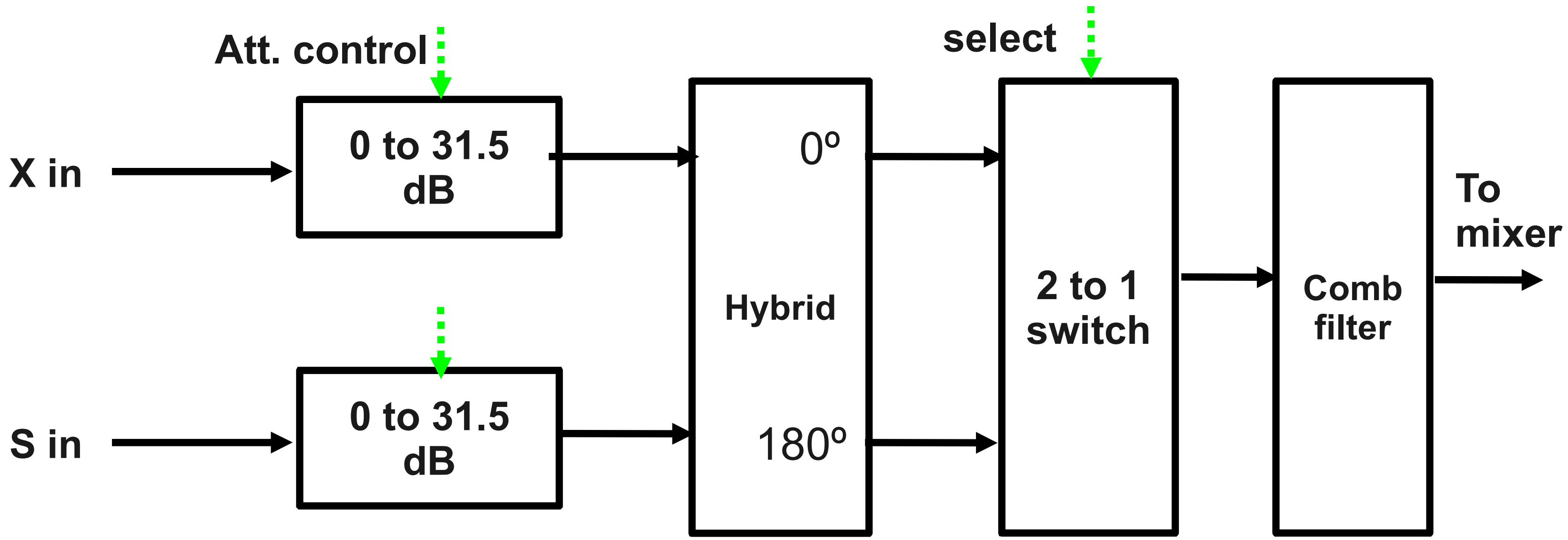
Spectrum of stripline signals



Orbit component compensation with sum signal

- Orbit offset and gain asymmetry produce revolution harmonics in the x/y signal.
- The component is sampled into a DC value.
- It is filtered out by The feedback FIR filter.
- However if the offset is large it can saturate the input ADC and lose useful spectrum.
- Two approaches:
  - Notch filter with a one-turn delay.
  - Gain adjustment of individual blades.
- Our approach is equivalent to the latter.
- Low cost and works for light source because the DC orbit is well controlled and does not change during run period.

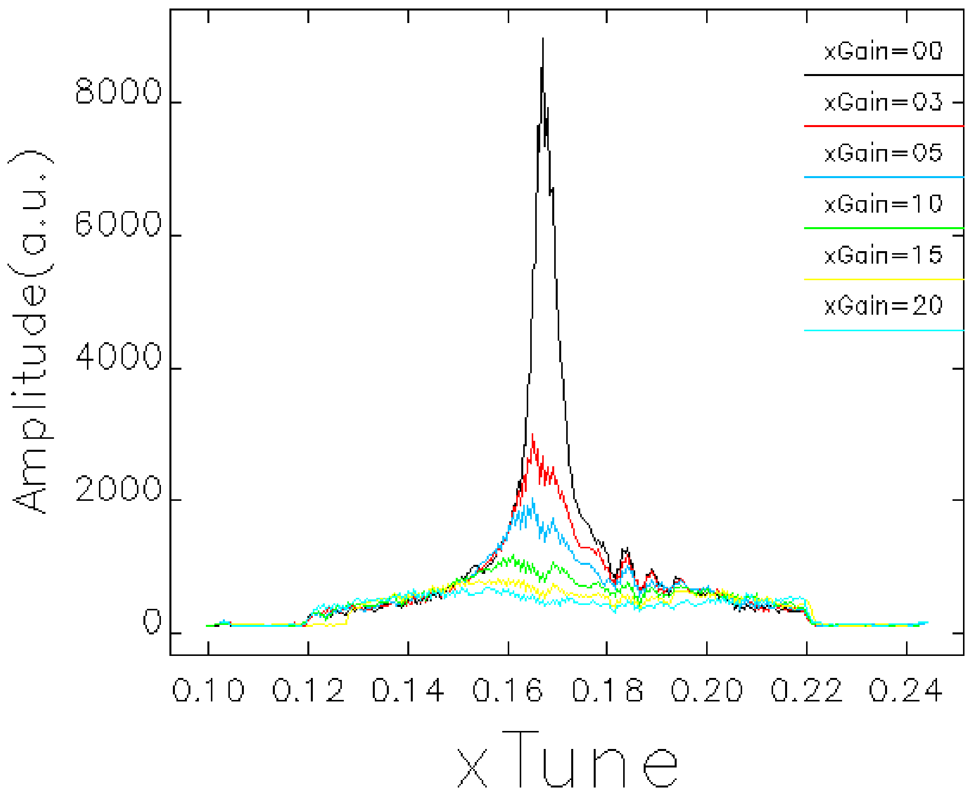
Orbit component compensation circuit

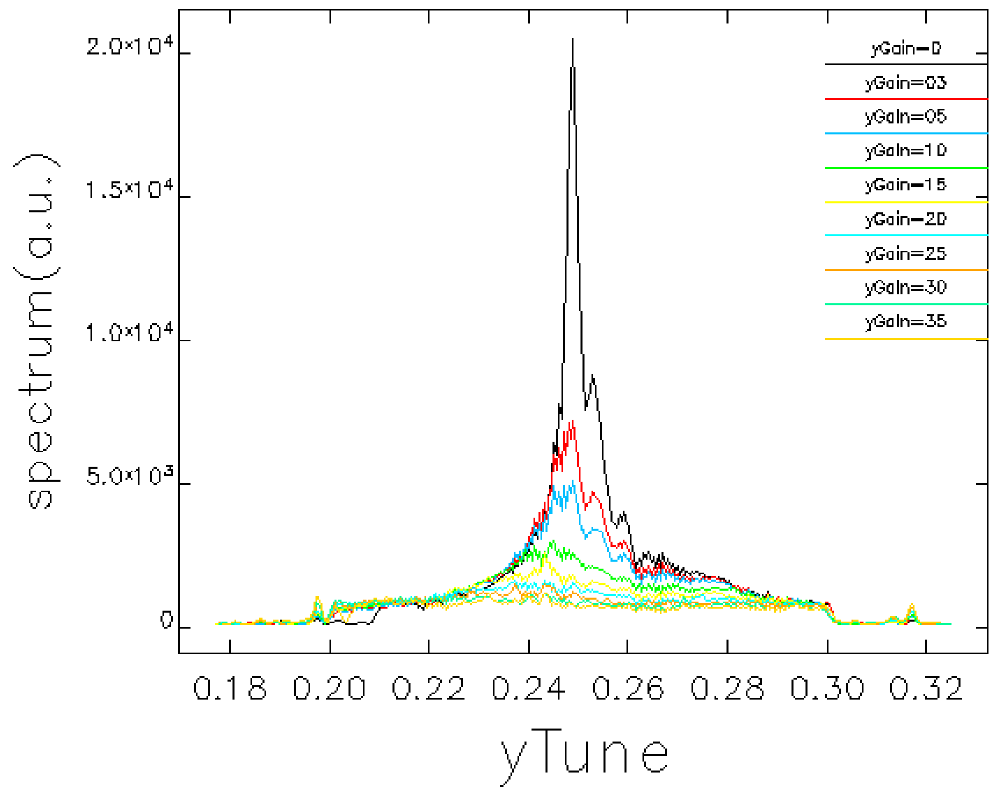


Independent bunch-by-bunch tune measurement system

- Separate processor: Altera Stratix-II DSP kit.
- Shared front-end and clock source.
- Recorders for raw ADC sample waveforms.
- Turn-by-turn waveforms.
- FFT waterfall waveforms.
- Event receiver interface that allows synchronization of the tune acquisition with many events such injection, booster extraction, top-up injection, etc.
- For feedback system diagnostics and front-end tuning.
- Can be used for tune measurement and other studies, such as fast ion and e-cloud, etc.

Check damping effect with tune-gain scan

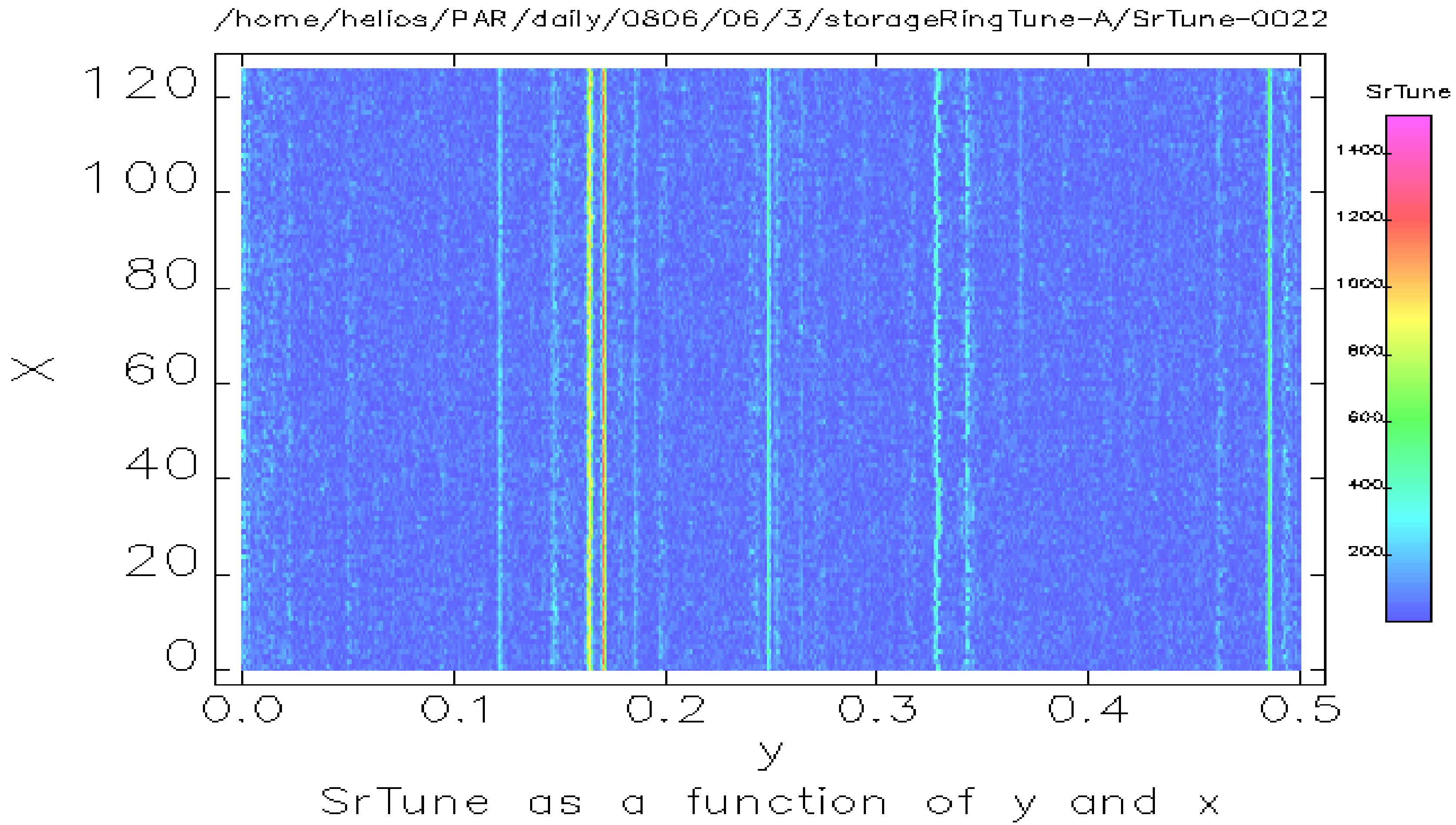




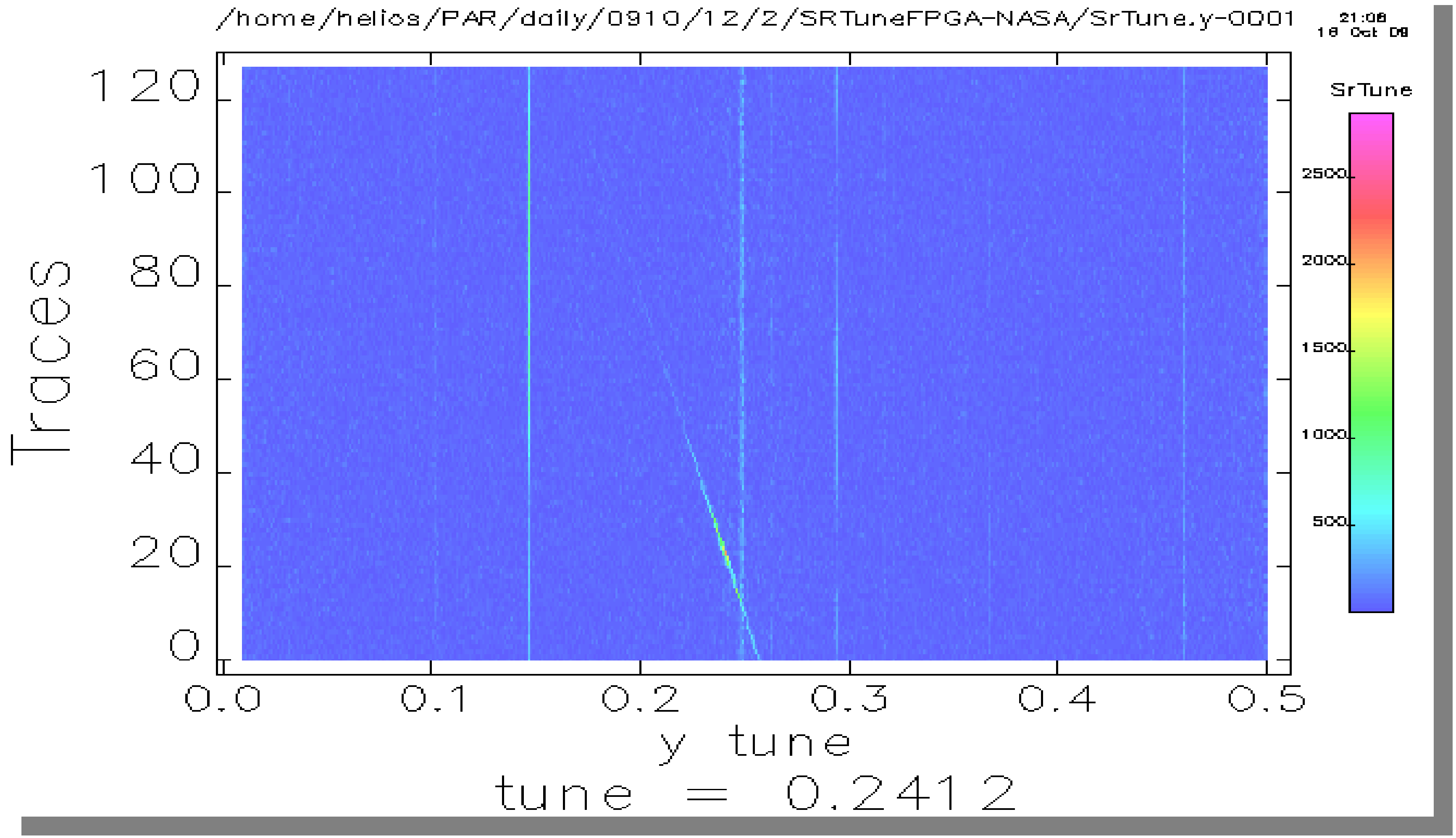
Noise analysis and reduction

- Noise signal contributes to the close-loop beam emittance. Reducing noises is essential.
- Noise analysis was performed using both an Agilent MXA signal analyzer and the FPGA-based tune measurement system.
- Identified most of the sidebands:
  - 40 Khz sidebands from faster correctors switching supplies.
  - 20KHz noise sidebands from the quads and sextupoles supplies. Could be directly coupled electronically.
  - Jitter in the sample clock, P0 and mixer LO clock source.
  - Noises generated in the FPGA electronics.
  - Many sidebands are aliased into multiple sidebands and hard to trace original source.
  - PS group has implemented filtering circuits to all fast corrector power supplies, which reduced noise spectrum by 20 dB.

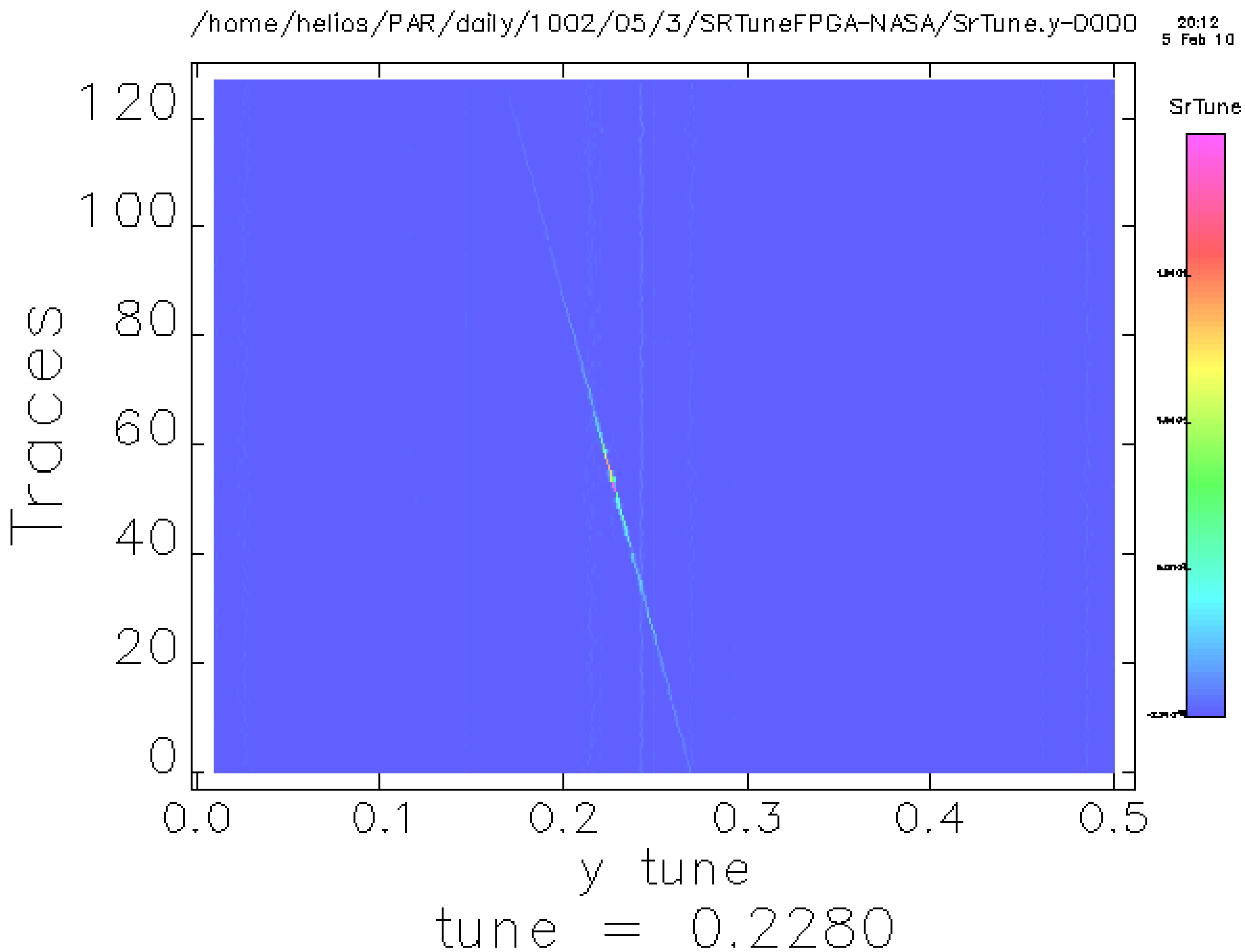
Beam spectrum taken earlier



Vertical tune spectrum before corrector upgrade

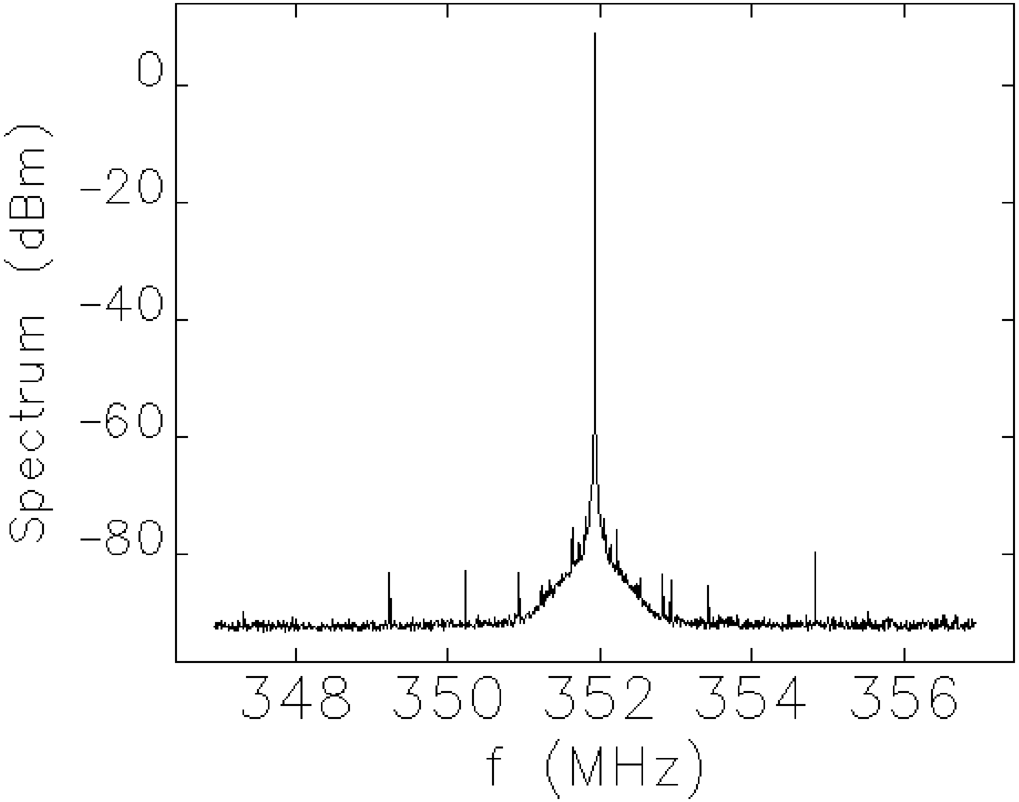


Vertical tune spectrum taken recently.



Clock source improvement

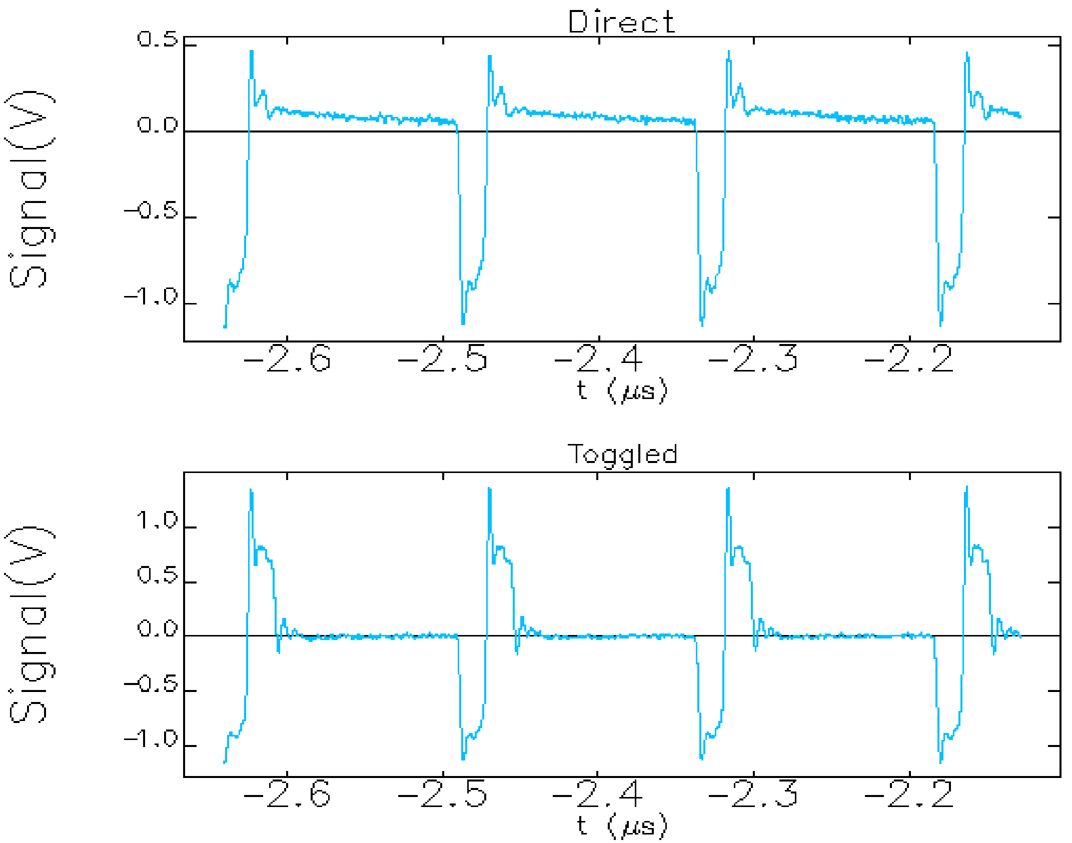
- Clock source cleanness directly impacts system performance and noise level.
- Compared two alternatives:
  - a 352 MHZ source transmitted by optic fibre from timing system
  - a source directly from RF system by coax cable
- The direct RF source is currently used.
- A 352-MHz CF and 1 MHz BW BP filter was added to remove a 1 MHz side-band in the source signal.
- An upgrade clock and P0 cleaner circuit is being developed, which will substantially reduce jitters[1].



[1]Tony Scaminaci

AC coupling effect of the DAC out and drive circuits

- The FPGA DAC output is transformer- coupled.
- There is baseline shift when the data rate is low.
- We added a toggle option in the DAC output processing to eliminate DC level drift.
- Useful for single bunch or 24 bunch fill pattern.
- Does not work if all the buckets are sampled and processed.

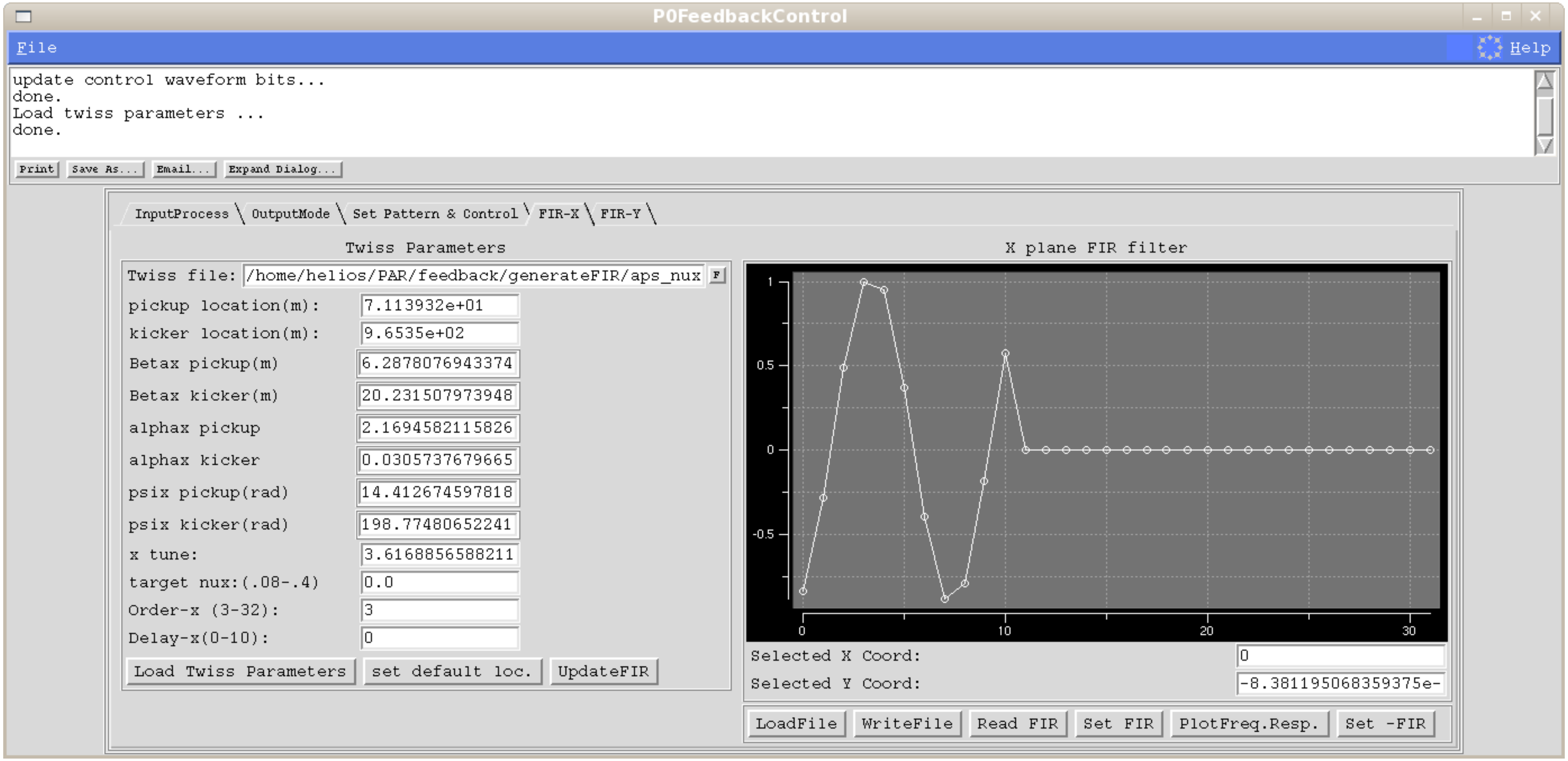


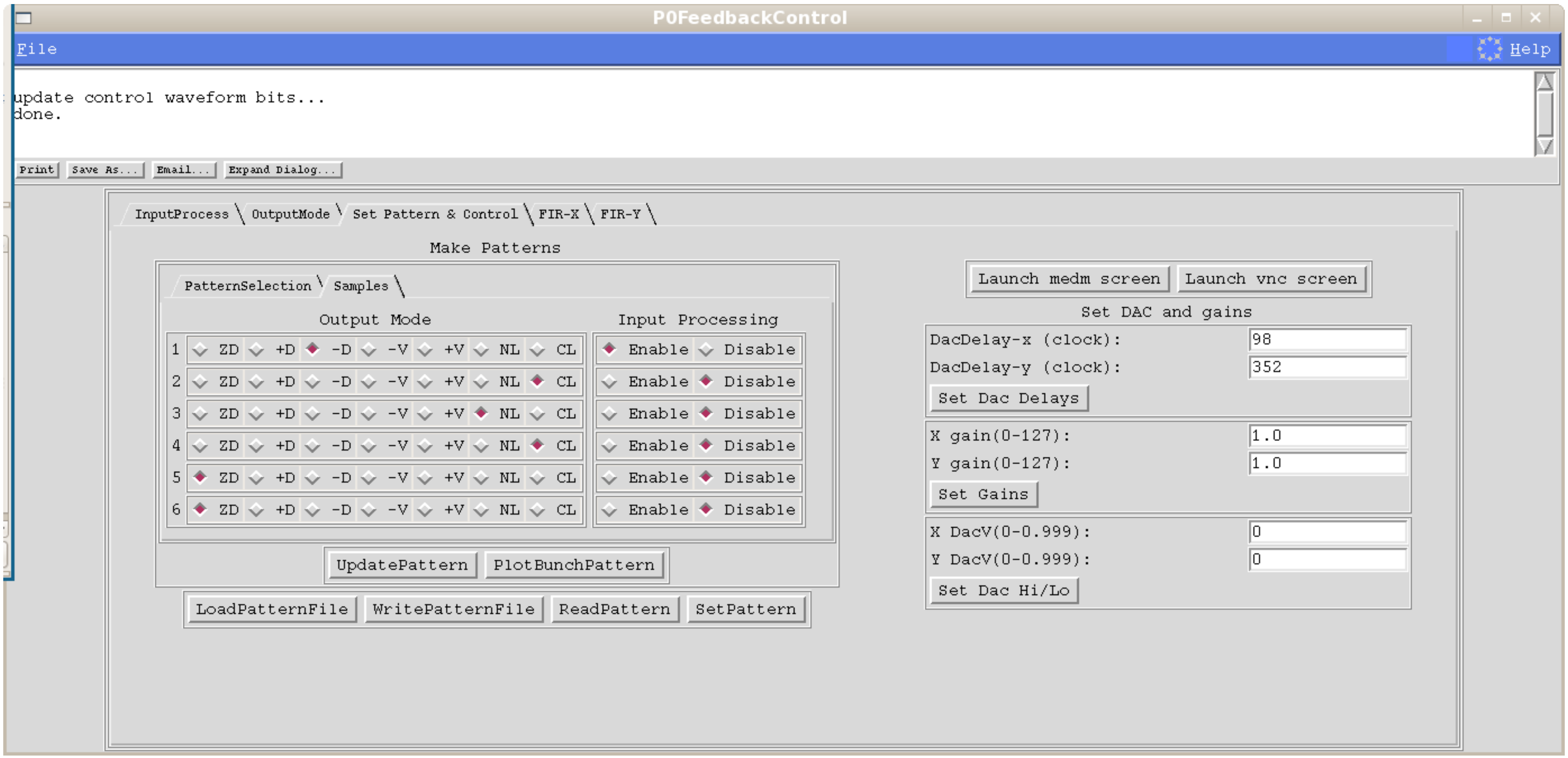
High level control application

A GUI application is developed for system control:

- Directly reads parameters from a lattice file
- Loads and saves filter files.
- Plot frequency response.
- Also provide bunch pattern, gain and other controls functions.

High level control application




P0FeedbackControl
File
Help
update control waveform bits...
done.
Print
Save As...
Email...
Expand Dialog...
InputProcess
OutputMode
Set Pattern & Control
FIR-X
FIR-Y
Make Patterns
PatternSelection
Samples
Output Mode
Input Processing
ZD +D -D -V +V NL CL
Enable Disable
UpdatePattern
PlotBunchPattern
LoadPatternFile
WritePatternFile
ReadPattern
SetPattern
Launch medm screen
Launch vnc screen
Set DAC and gains
DacDelay-x (clock): 98
DacDelay-y (clock): 352
Set Dac Delays
X gain(0-127): 1.0
Y gain(0-127): 1.0
Set Gains
X DacV(0-0.999): 0
Y DacV(0-0.999): 0
Set Dac Hi/Lo


GRAINGER
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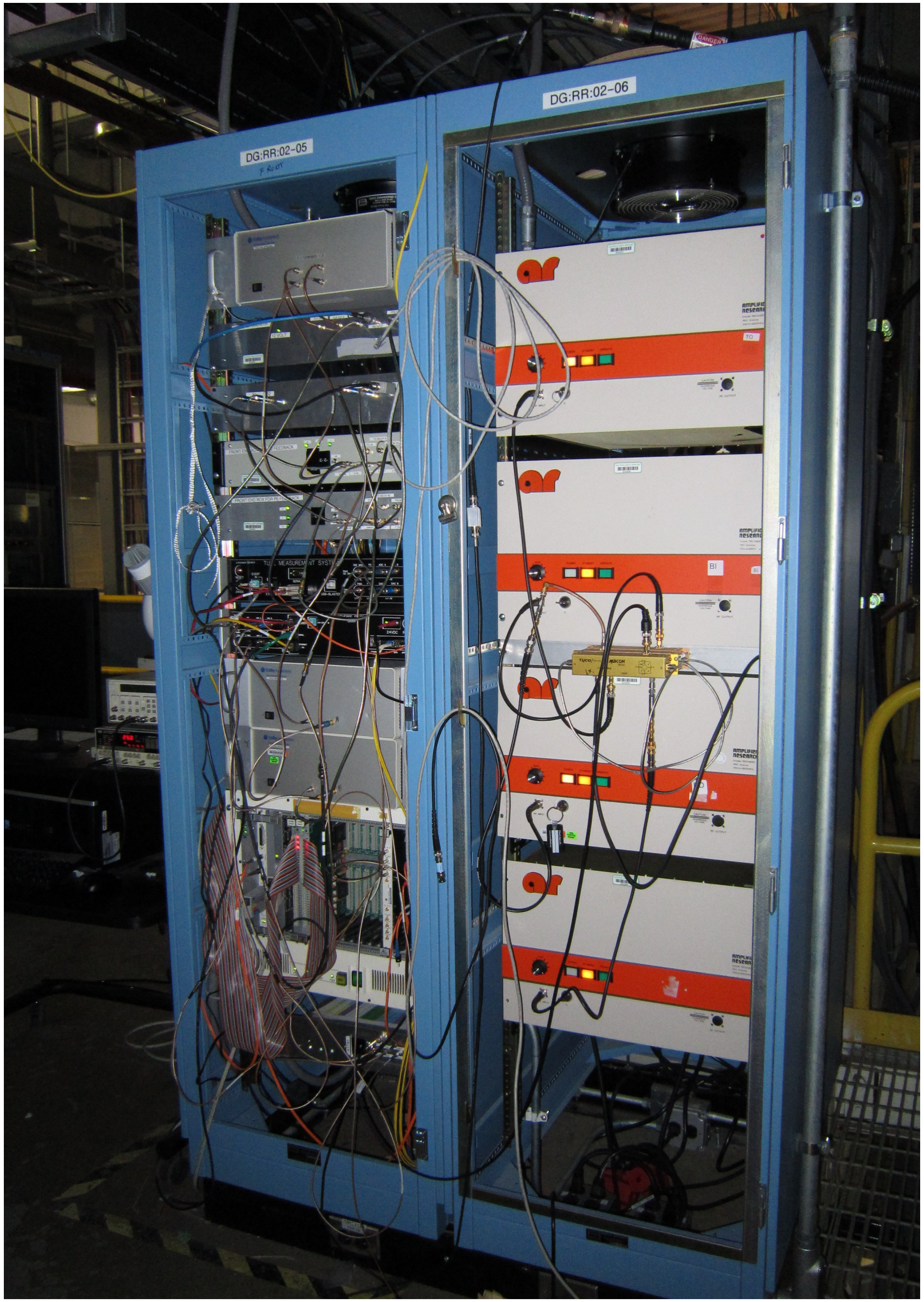
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Further upgrade plan

- Further reduce system noise level.
- Explore adaptive filter that deal with tune shift issue.
- Gain control for different bunch charge.
- Increase system bandwidth to full 352 MHz.
- Apply the system to APS upgrade.

References

- T. Nakamura, private communications.
- Eric Plouviez , et al. “Bunch by bunch transverse feedback development at ESRF”, EPAC08.
- C.-Y. Yao, et al. “An FPGA-based bunch-to-bunch feedback system at the Advanced Photon Source,” PAC07.
- T. Nakamura, “Single-loop two-dimensional transverse feedback for Photon Factory,” EPAC06.