Wide Bandgap (WBG) Semiconductor Power Devices for Switching and RF Power Supplies

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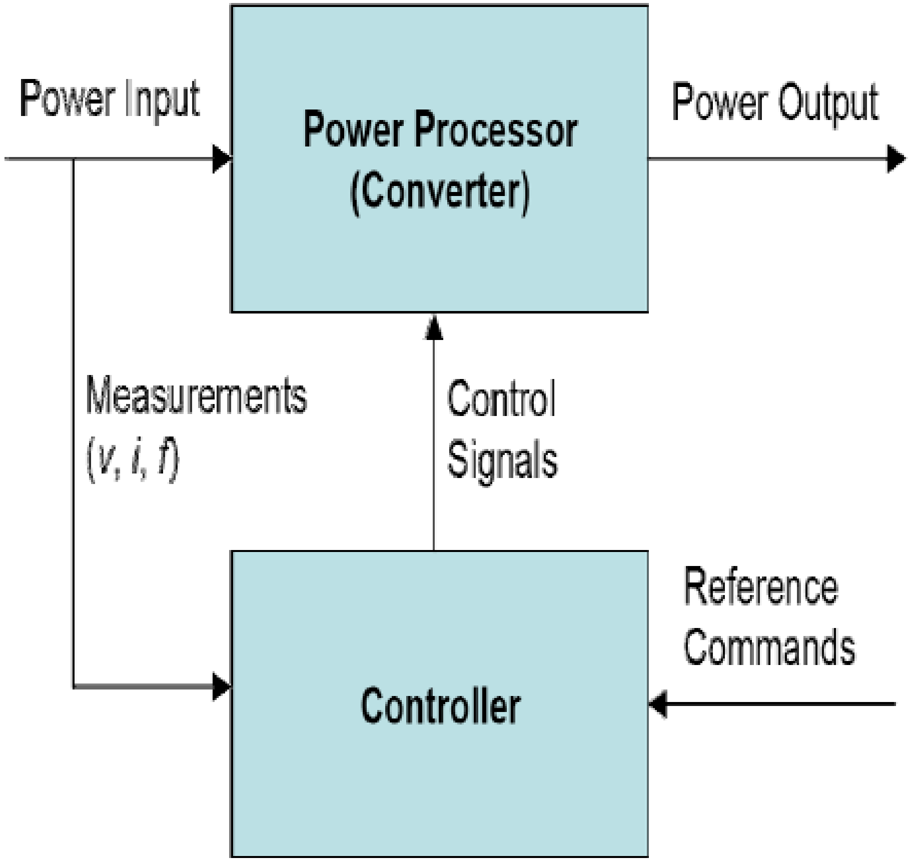
Argonne National Laboratory

ASD Seminar Presented at:

Advanced Photon Source

September 19, 2014

Power Semiconductor Switch in a Power Converter



Power Input

Power Processor (Converter)

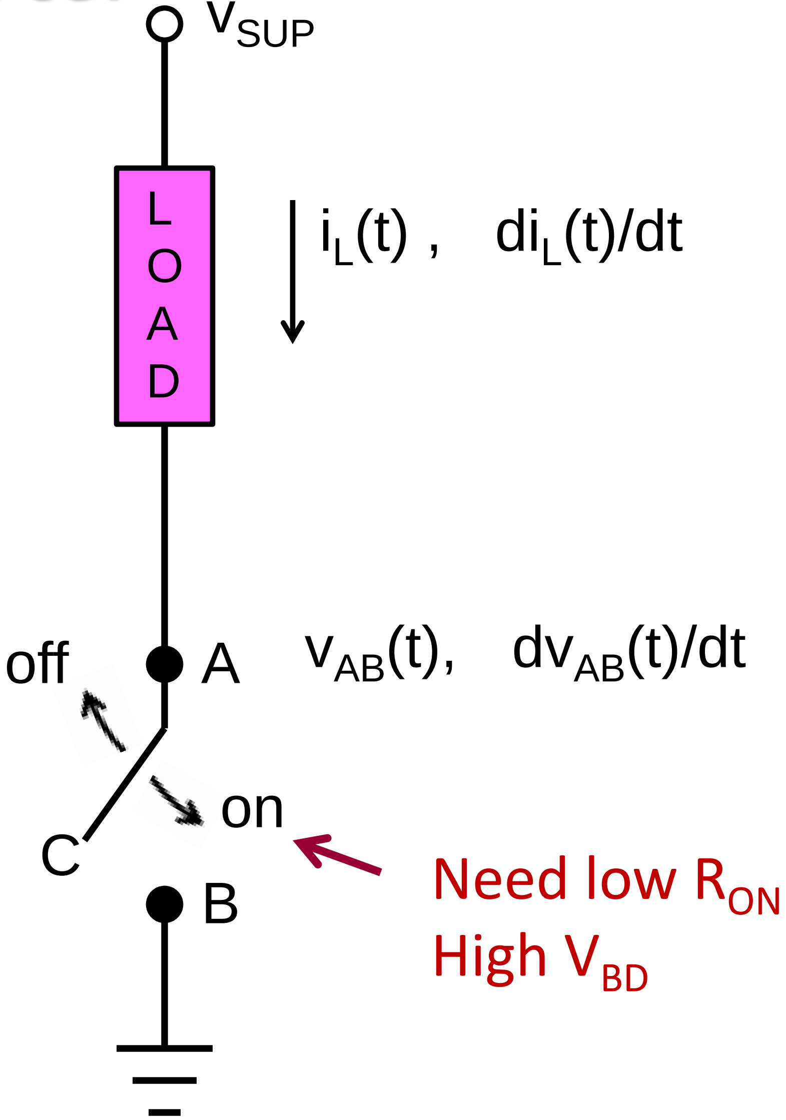
Power Output

Measurements (v, i, f)

Control Signals

Controller

Reference Commands

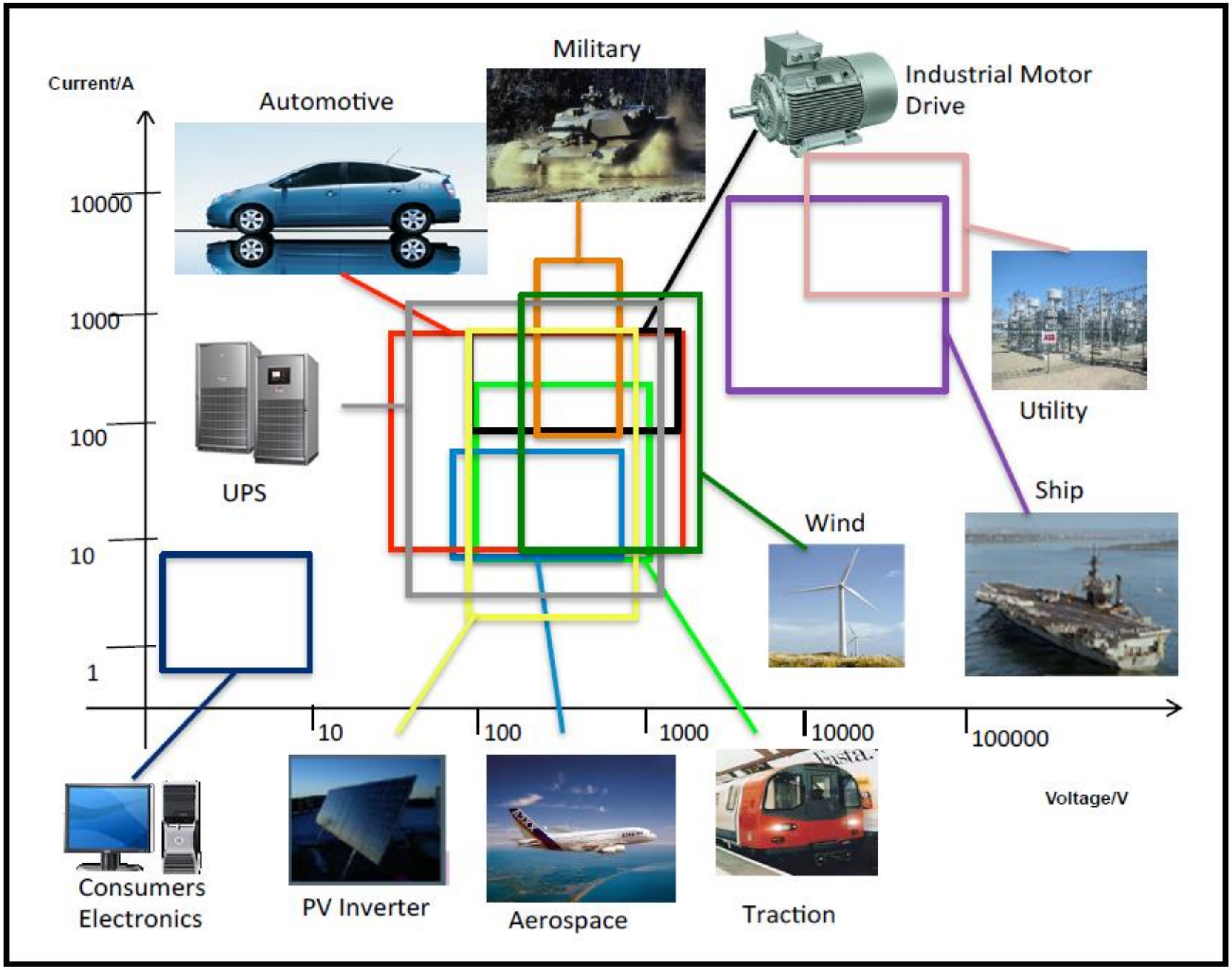


Need low R_{ON}

High V_{BD}

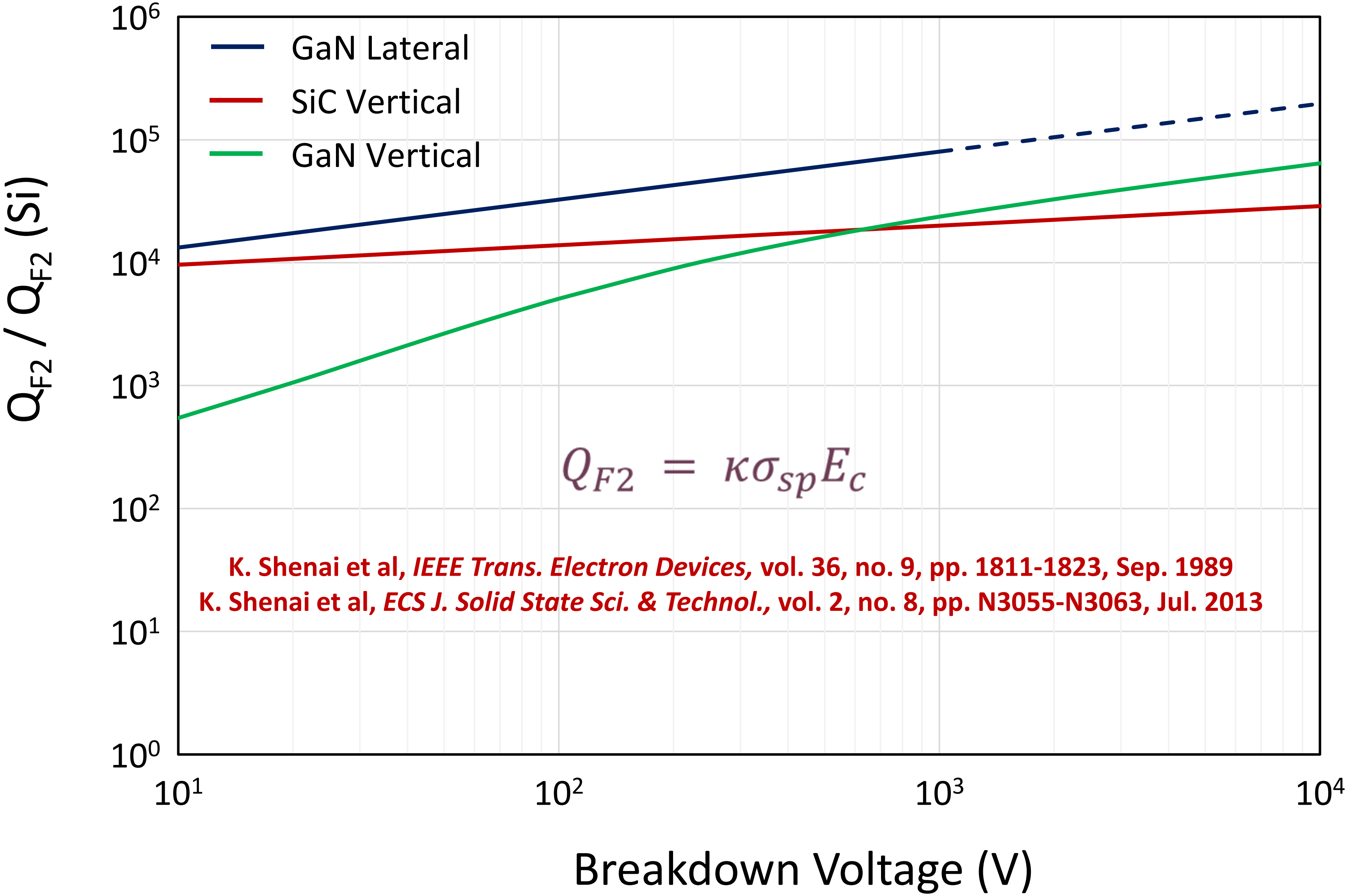
What is the Role of Power Electronics in the Emerging 21st Century Energy Economy?

Power Electronics Applications



Power Electronics Industry Consortium (PEIC)

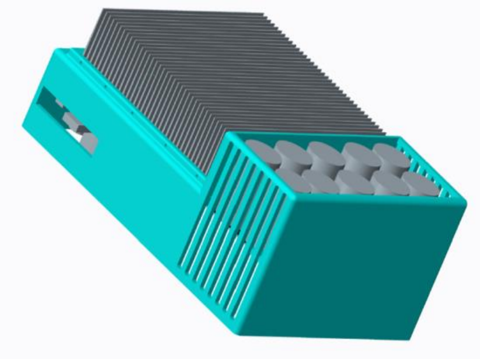
Why Wide Bandgap (WBG) Semiconductors?



$$Q_{F2} = \kappa \sigma_{sp} E_c$$

K. Shenai et al, *IEEE Trans. Electron Devices,* vol. 36, no. 9, pp. 1811-1823, Sep. 1989

K. Shenai et al, *ECS J. Solid State Sci. & Technol.,* vol. 2, no. 8, pp. N3055-N3063, Jul. 2013



Si is the industry workhorse

WHY WBG?

Increased Energy Efficiency

If there is no cost and reliability penalty

Smaller Converter Profile

Requires higher converter switching frequency and system integration

Reduced Thermal Budget

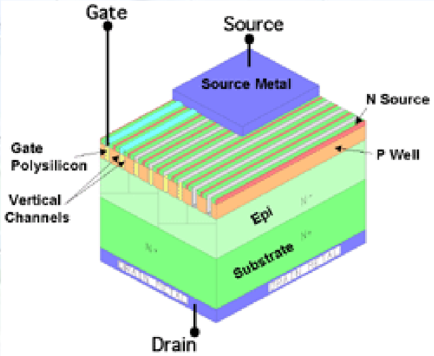
High-temperature semiconductor and improved thermal management

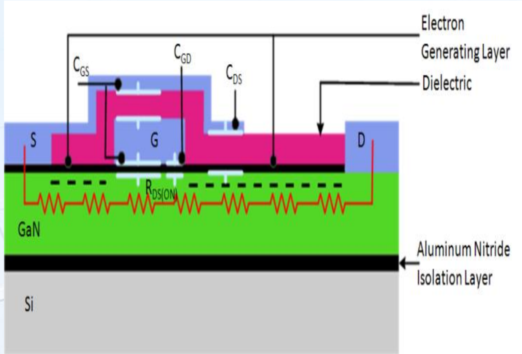
Wide bandgap (WBG) semiconductors, such as SiC and GaN devices, offer superior electrical and thermal performances compared to silicon

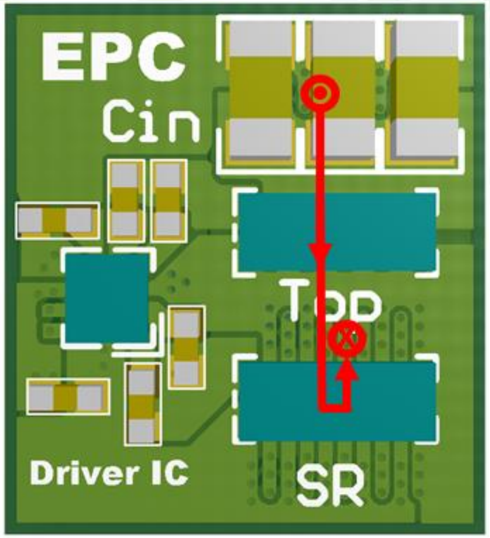
K. Shenai *et al,* "Optimum Semiconductors for High-Power Electronics," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1811-1823, September 1989.

Power SOC

Collaborator:
Alex Lidow, EPC

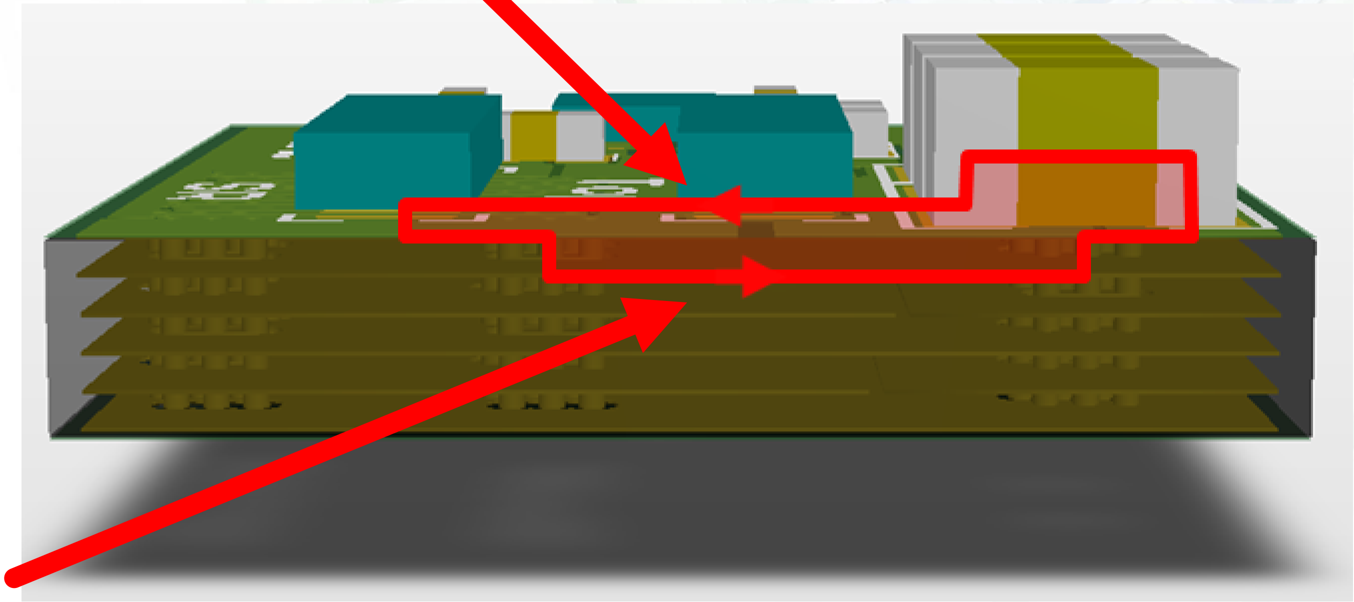


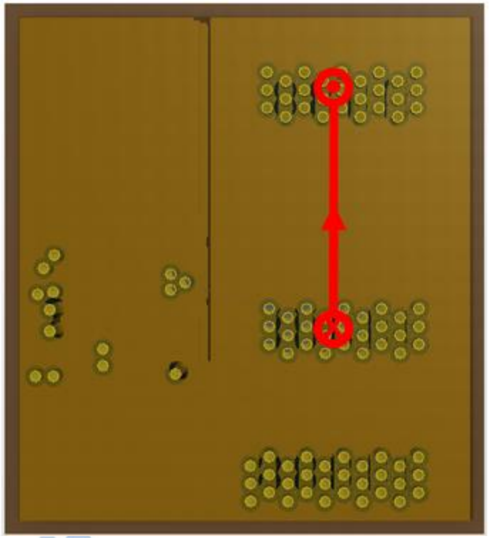




Top View

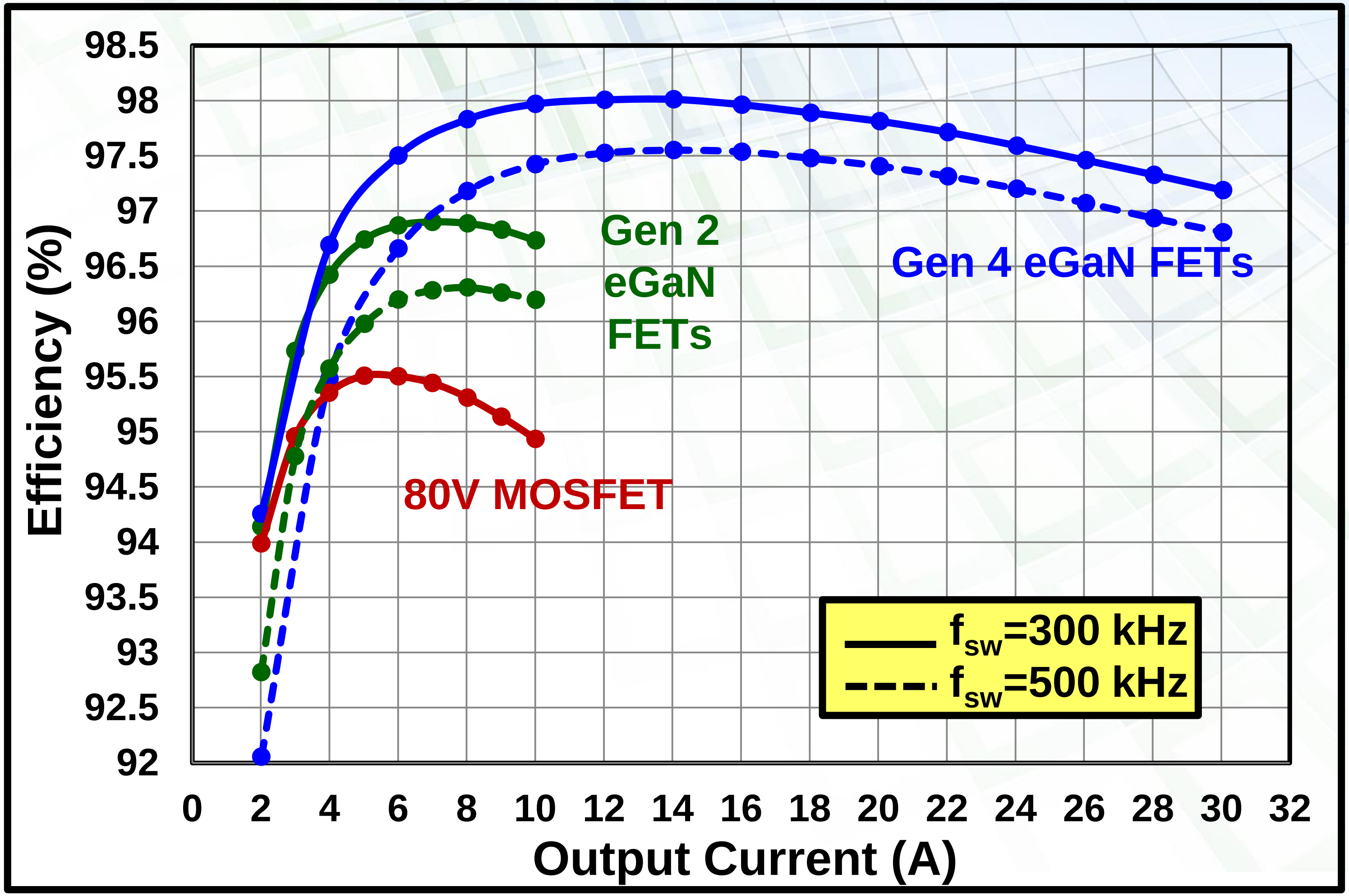
Side View





Top View
Inner Layer 1

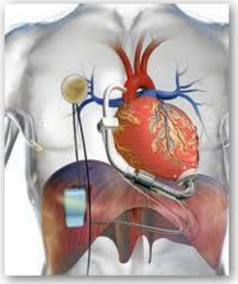
eGaN™ Battery Charger



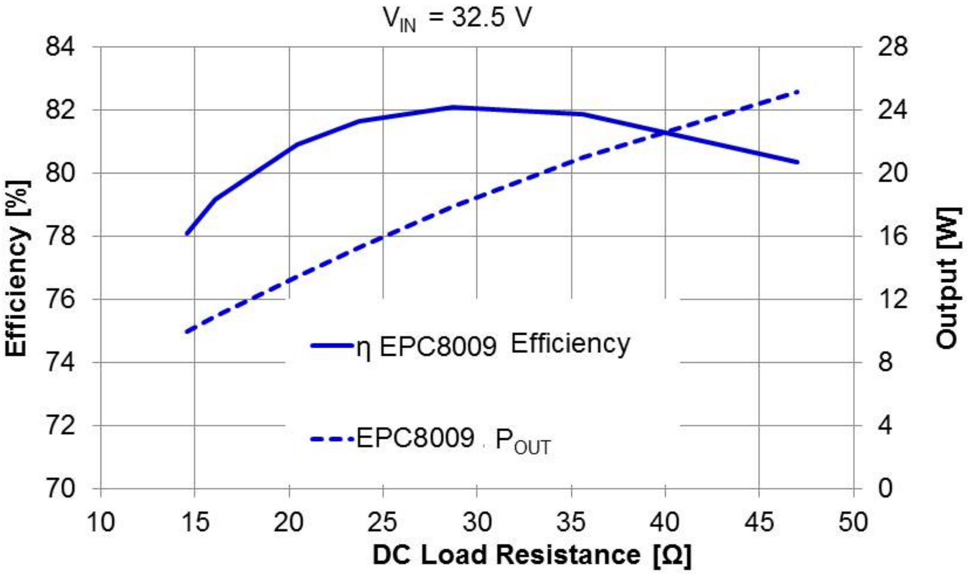
V_{IN}=48 V V_{OUT}=12 V

Why Wireless Energy?

- Mobile device charging
  - Convenience
  - Extended battery life
- Medical Implants
  - Quality of life improvement
  - Life extender
- Hazardous environment systems
  - Explosive atmosphere
  - Corrosive locations
  - High Voltage



Fixed Supply voltage, DC Load Resistance varied



Need to further:

- improve efficiency
- increase transmission range
- reduce cost

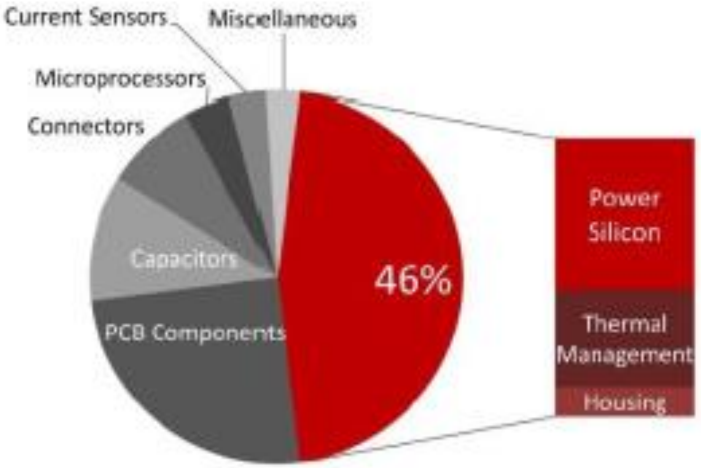
DoE's EV Everywhere

Electric Drive System 2022 Targets

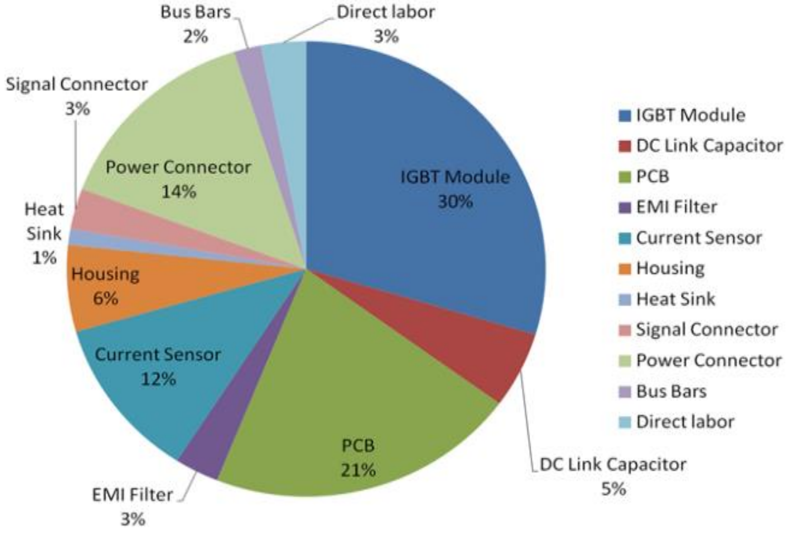
		Current Status	Target
System Cost	$/kW	30	8
Specific Power	kW/kg	1.1	1.4
Power Density	kW/L	2.6	4.0
Peak Efficiency	%	90	94

Vehicle Charging 2022 Targets

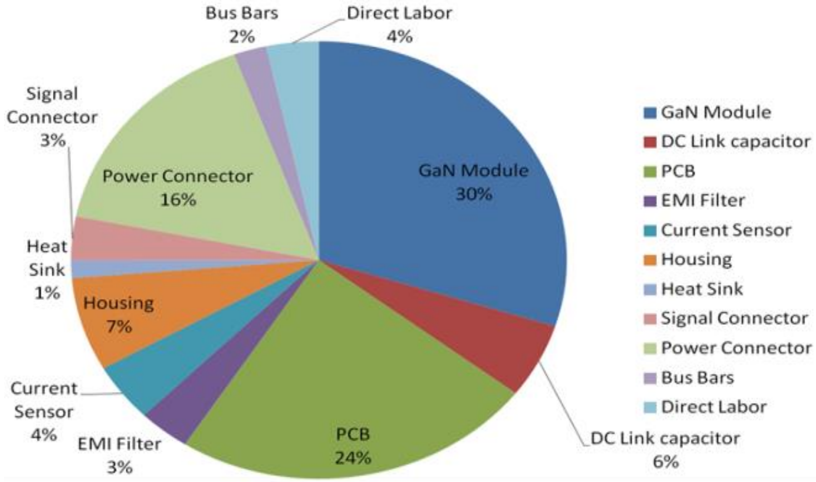
		Current Status	Target
Charger Cost	$/kW	150	35



Synthesis Partners LLC., July 2011



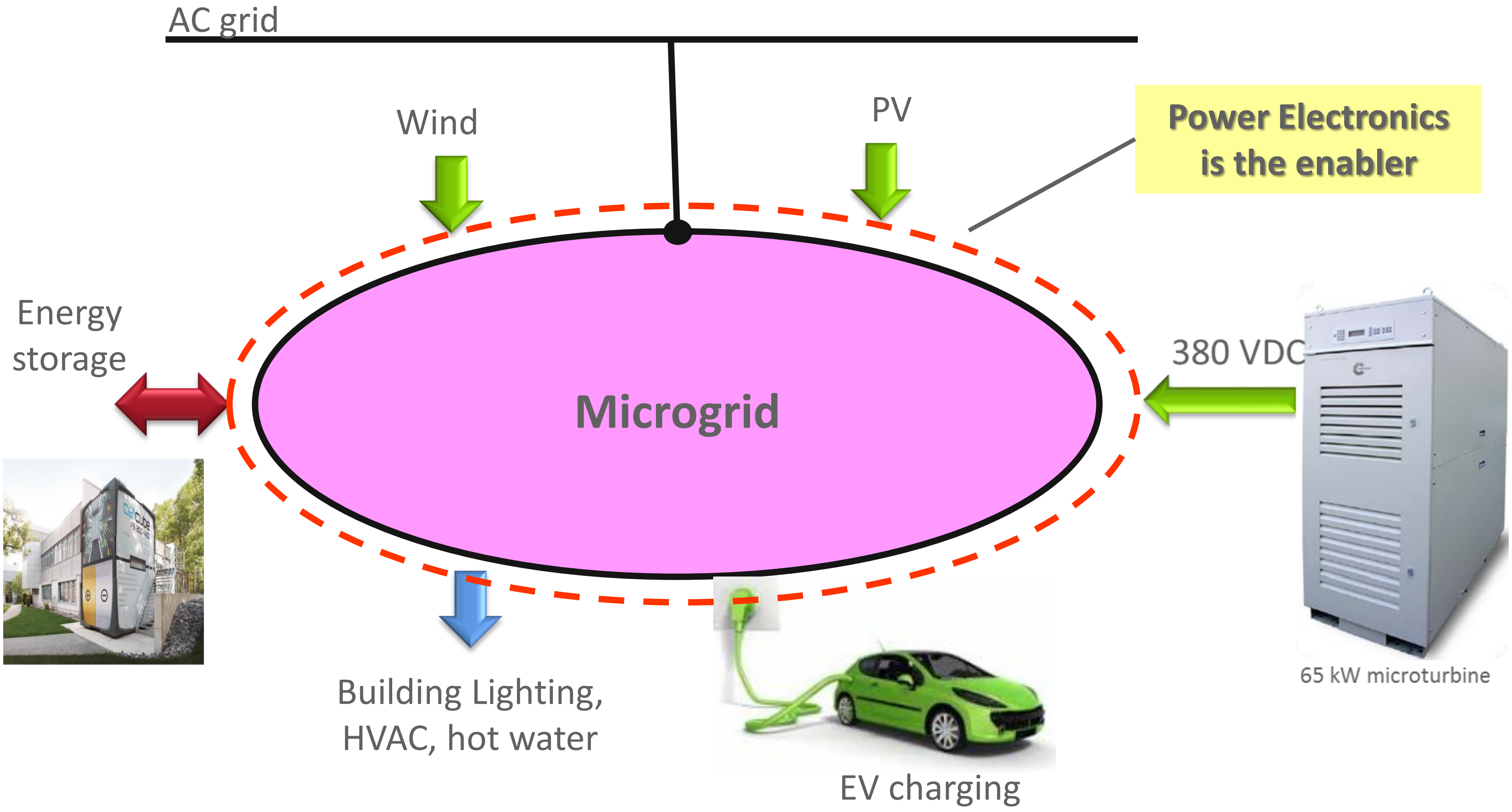
Production Cost	468.6
$/kW	7.94



Production Cost	416.0
$/kW	7.05

http://energy.gov/sites/prod/files/2014/04/f15/2013_apeem_report.pdf

Hybrid Microgrid



AC grid

Wind

PV

Power Electronics is the enabler

Energy storage

Microgrid

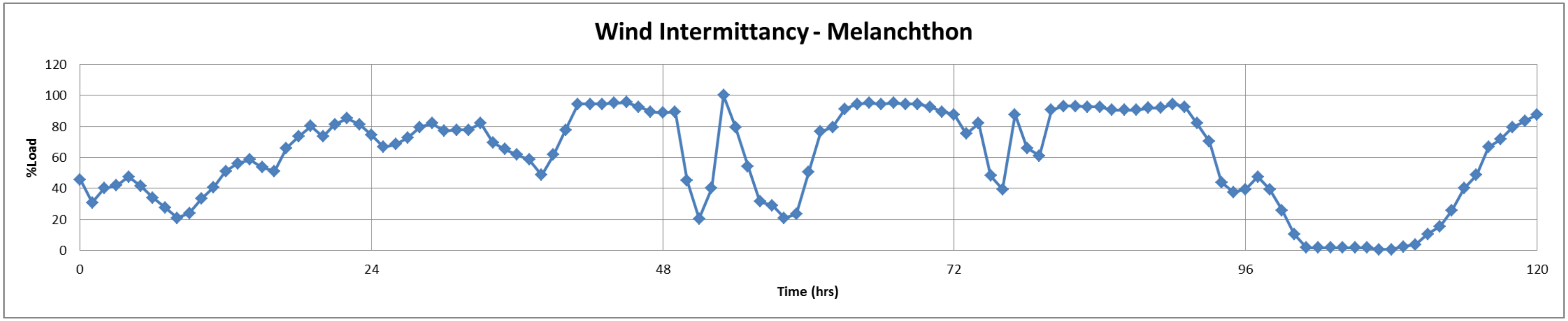
380 VDC

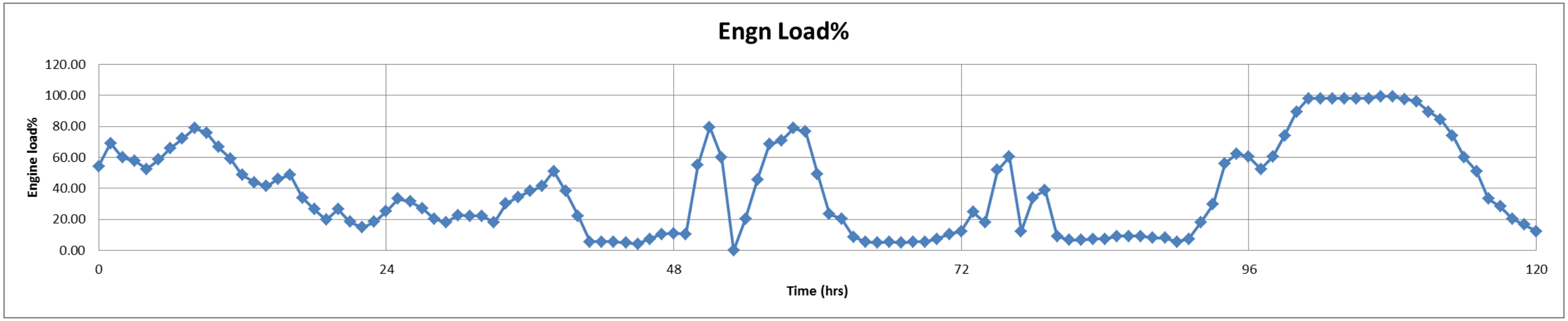
65 kW microturbine

Building Lighting, HVAC, hot water

EV charging

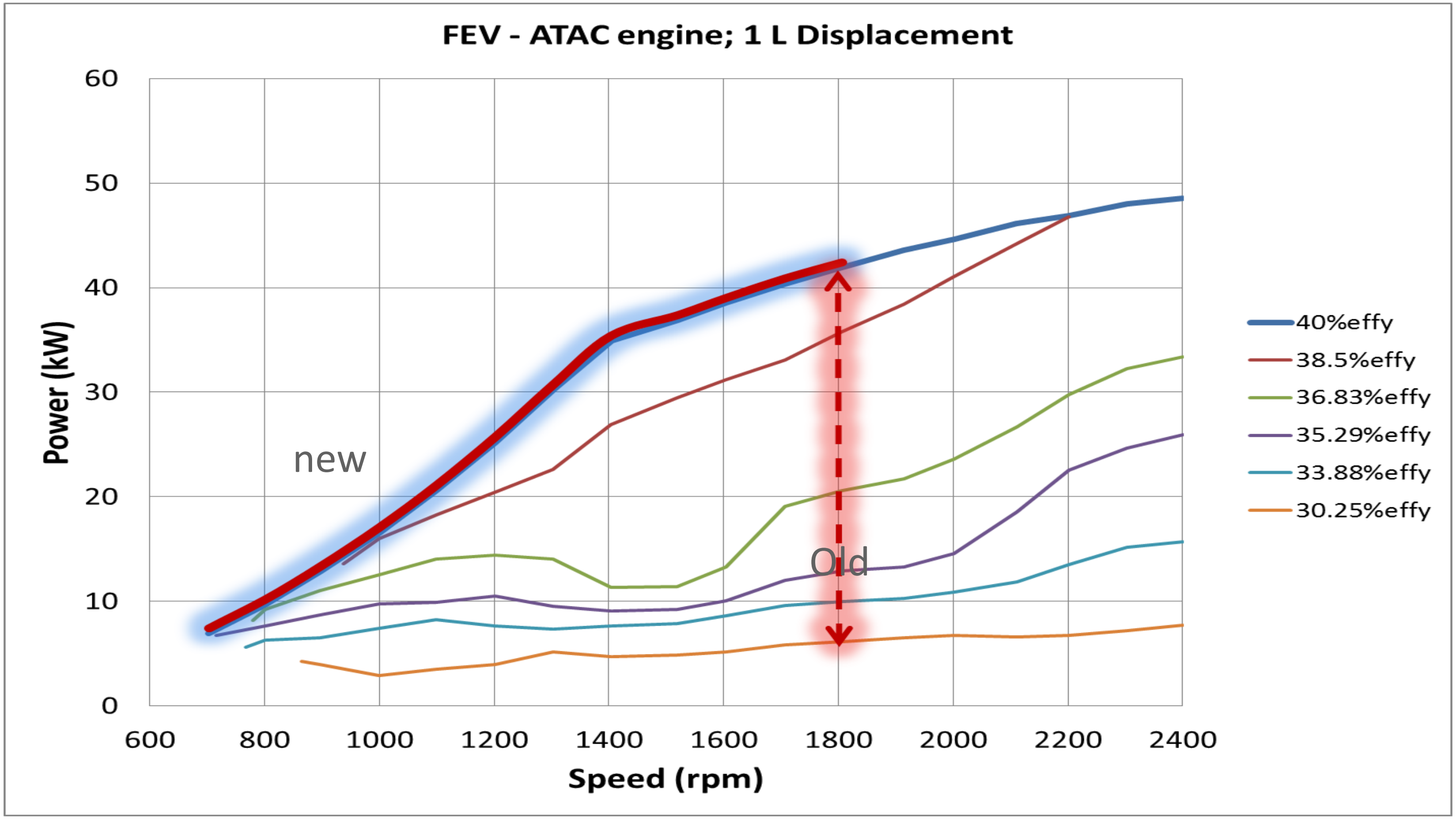
Firming Wind Power With Gas Generator

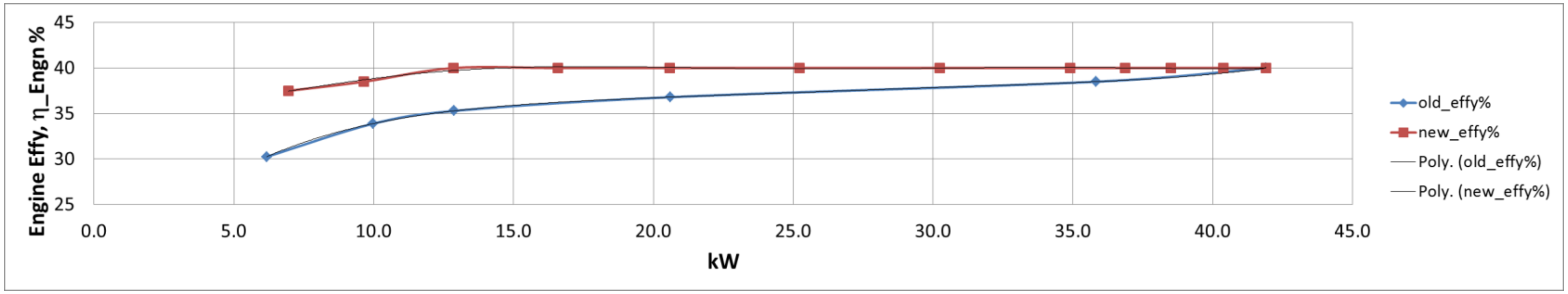




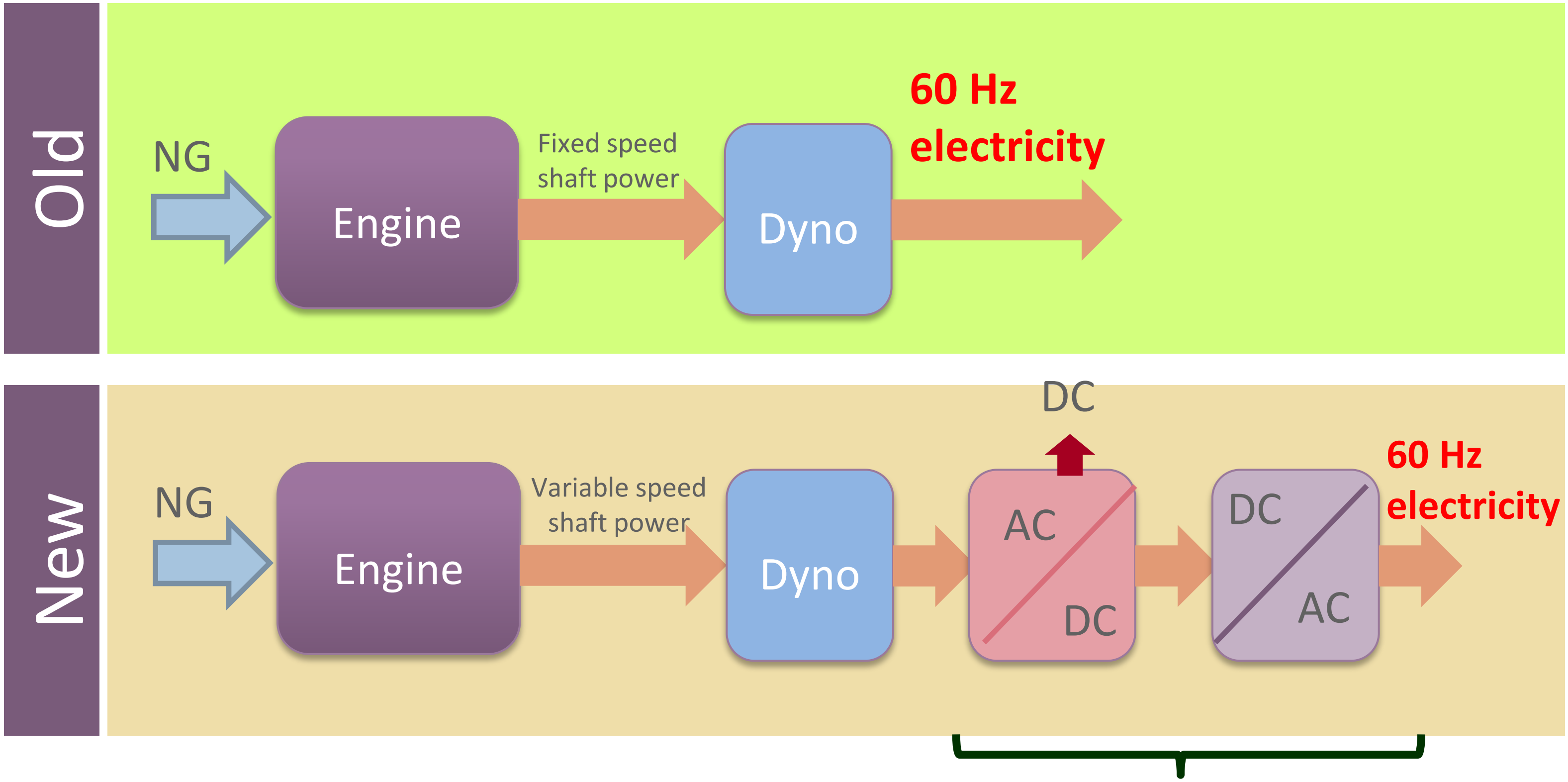
$$\text{net effy} = \frac{\sum_i Power_i \cdot \Delta t_i}{\sum_i \dfrac{Power_i \cdot \Delta t_i}{\eta_i}}$$

Breakthrough solution to deal with variable loads





Old school vs. New school



Old

NG

Engine

Fixed speed shaft power

Dyno

60 Hz electricity

New

NG

Engine

Variable speed shaft power

Dyno

AC / DC

DC

DC / AC

60 Hz electricity

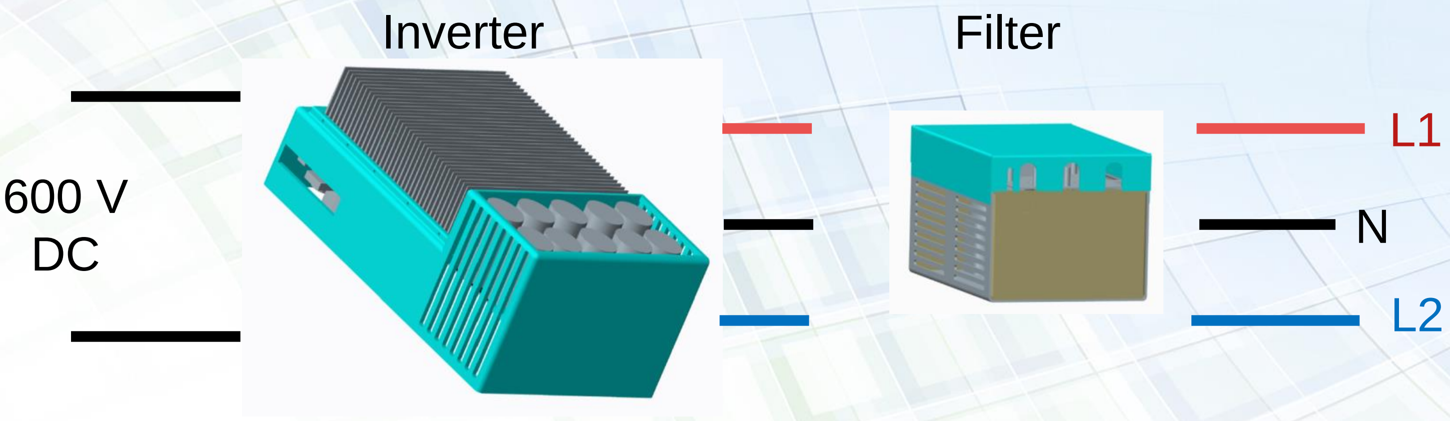
η_{net} %

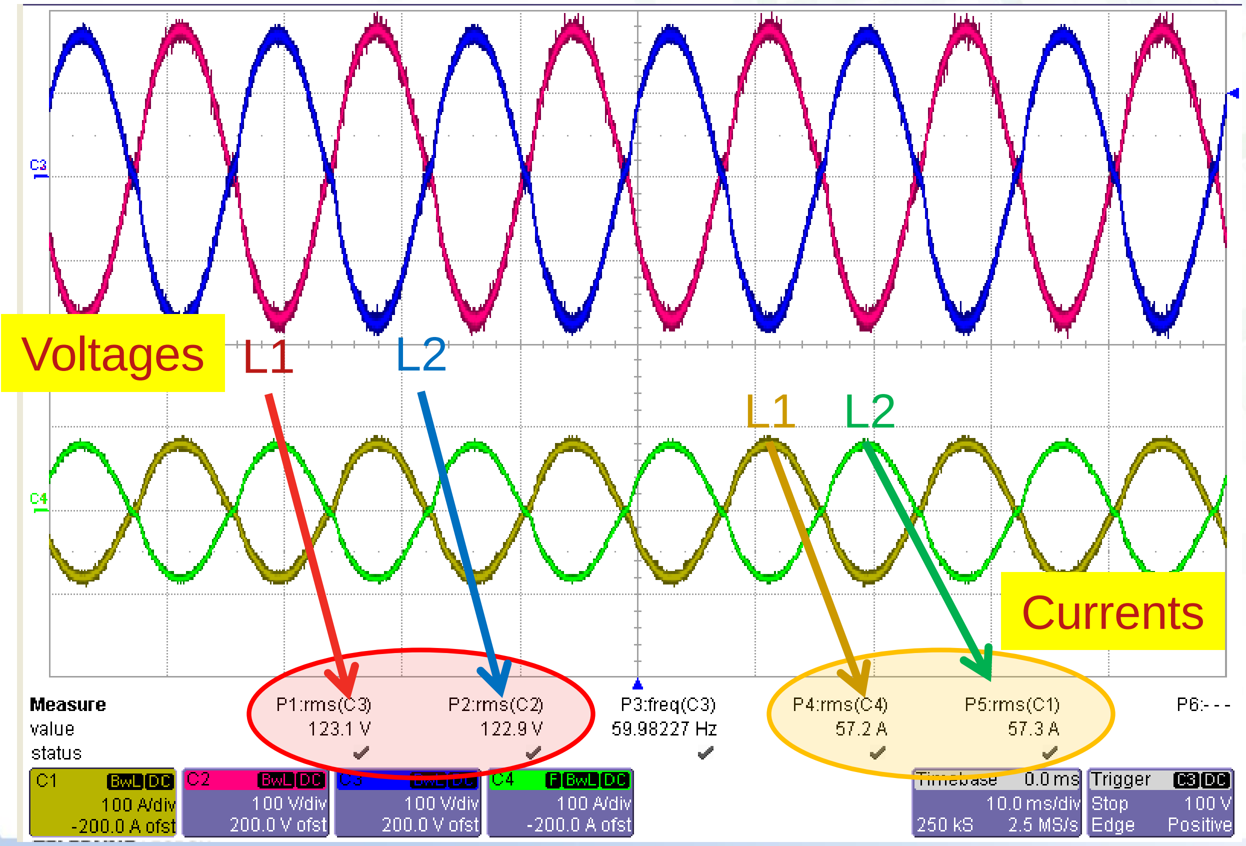
	η_{Conv} 100%	η_{Conv} 97%
Old	36.3	36.3
New	39.6	38.4
$\Delta\eta_{net}$ %	3.2%	2.1%

$$\eta_{net} = \eta_{Engn} \times \eta_{Dyno} \times \eta_{Conv}$$

- Need WBG power electronics to achieve these efficiency gains.
- Even better gains are possible for DC and variable speed drives

14 kW Air-Cooled SiC Split-Phase Inverter





Measure	P1:rms(C3)	P2:rms(C2)	P3:freq(C3)	P4:rms(C4)	P5:rms(C1)	P6:- - -
value	123.1 V	122.9 V	59.98227 Hz	57.2 A	57.3 A	
status	✓	✓	✓	✓	✓	

C1 BwL DC 100 A/div -200.0 A ofst

C2 BwL DC 100 V/div 200.0 V ofst

C3 BwL DC 100 V/div 200.0 V ofst

C4 F BwL DC 100 A/div -200.0 A ofst

Timebase 0.0 ms 10.0 ms/div 250 kS 2.5 MS/s

Trigger C3 DC Stop 100 V Edge Positive

Switching freq.: 20 kHz

Air flow: 300 CFM

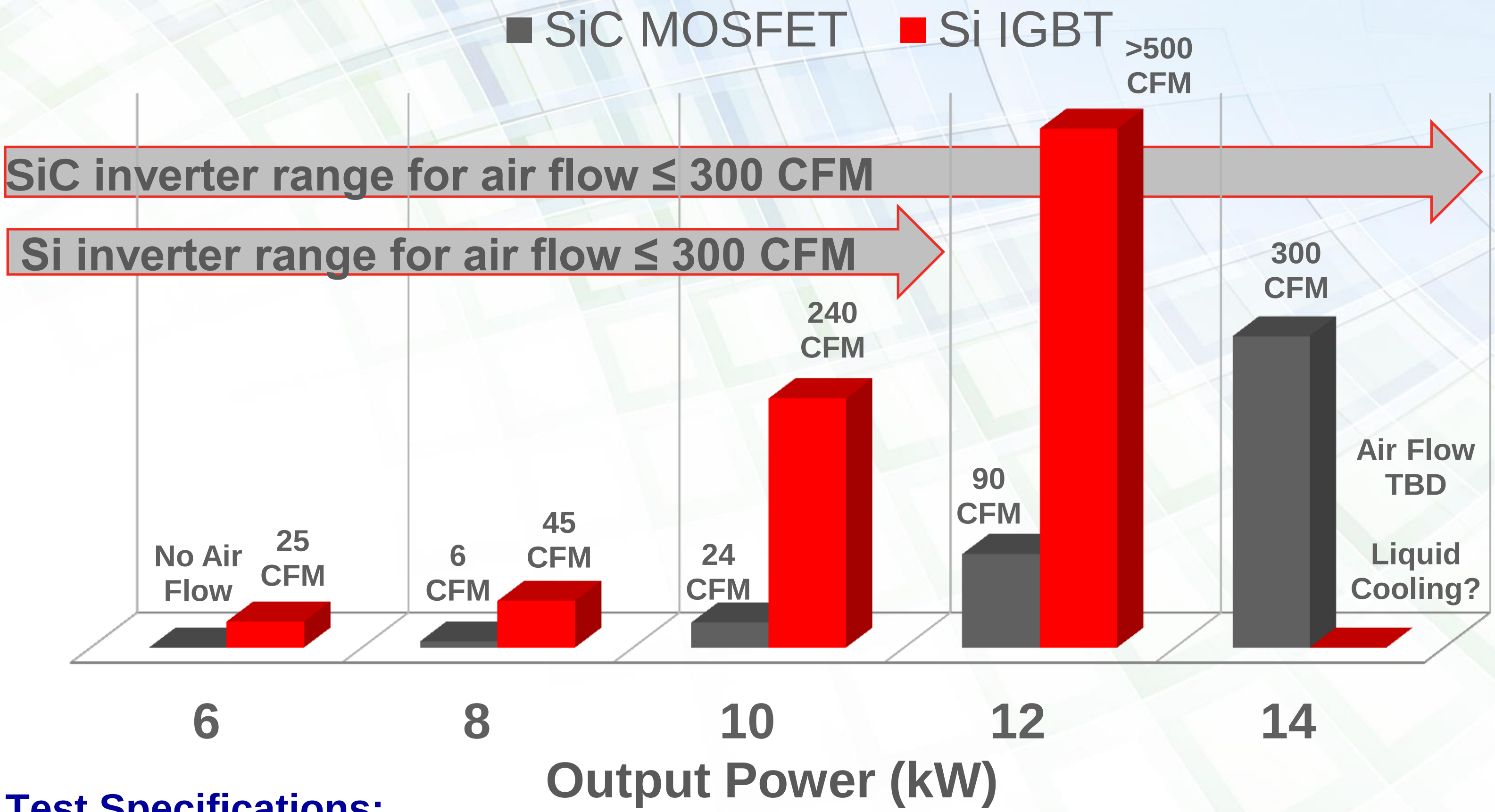
Junction temp.: 115 °C

Case temp.: 68 °C

Ambient temp.: 20 °C

Efficiency: 94%

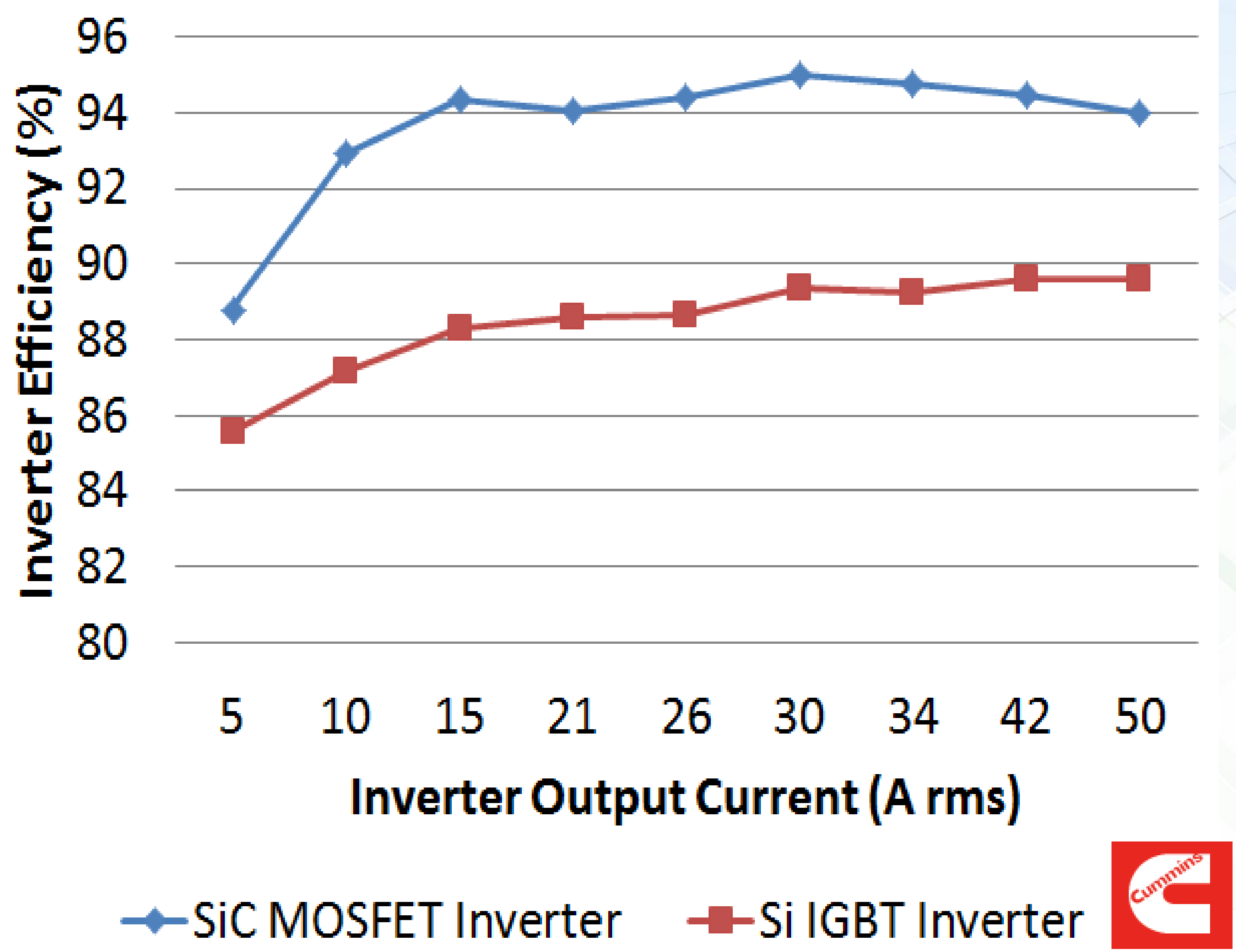
Air Flow vs Output Power for T_j = 115 °C



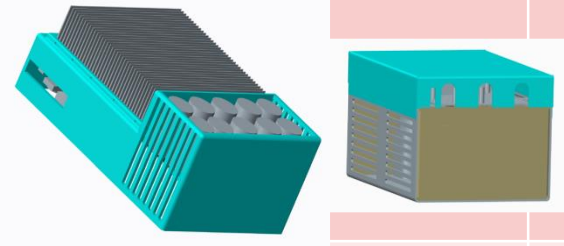
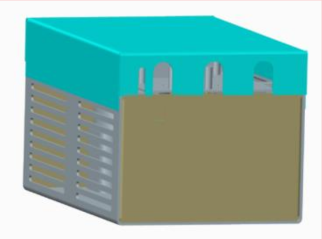
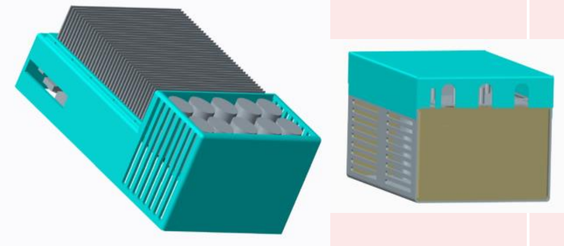
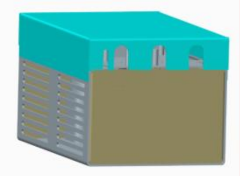
Test Specifications:

- 120/240 V, 60 Hz ac output
- 400 V DC input for 6 – 8 kW and 600 V DC input for 10 – 14 kW
- Balanced loading conditions
- Switching frequency: 20 kHz
- Room ambient: 20 °C
- Gate drives: SiC MOSFET v_{GS} = +20/–6 V, Si IGBT v_{GE} = +17/–9 V
- Temperature data recorded upon reaching thermal steady state of switches

Measured Inverter Efficiency

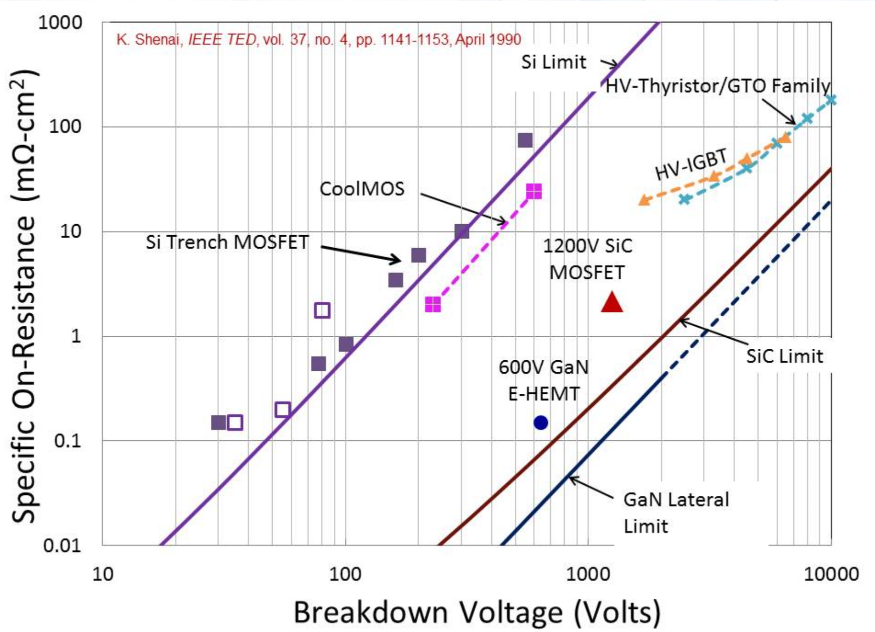


Design Options to Reduce System-Level $/kW

	OPTION 1 **Higher Power** **14 kW instead of 10 kW**	**OPTION 2** **Smaller Cooling** **@ 10 kW**	**OPTION 3** **Higher Frequency** **@ 8 kW**
Si Inverter	10 kW @ 90% efficiency 	240 CFM 	20 kHz switching 
SiC Inverter	14 kW @ 94% efficiency 	24 CFM 	50 kHz switching 
	20 kHz switching freq. ≤ 300 CFM Air Flow 115 °C junction temperature **40% more power (kW↑)** **4% more efficiency**	20 kHz switching freq. 115 °C junction temperature **90% lesser cooling ($↓)**	**Estimated 30% reduction in filter cost and size ($↓)**

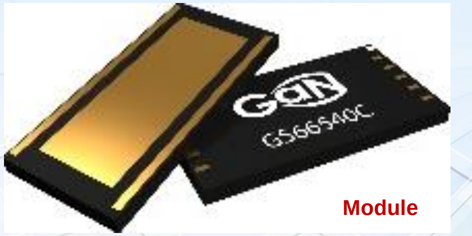
All options reduce: $$\frac{\text{Total System Cost (\$)}}{\text{Output Power (kW)}}$$

Lateral GaN Power Transistors – Emerging Breakthrough Technology



Recommend R&D with:

600V/200A single-chip and 600V/1000A module from GaN Systems.

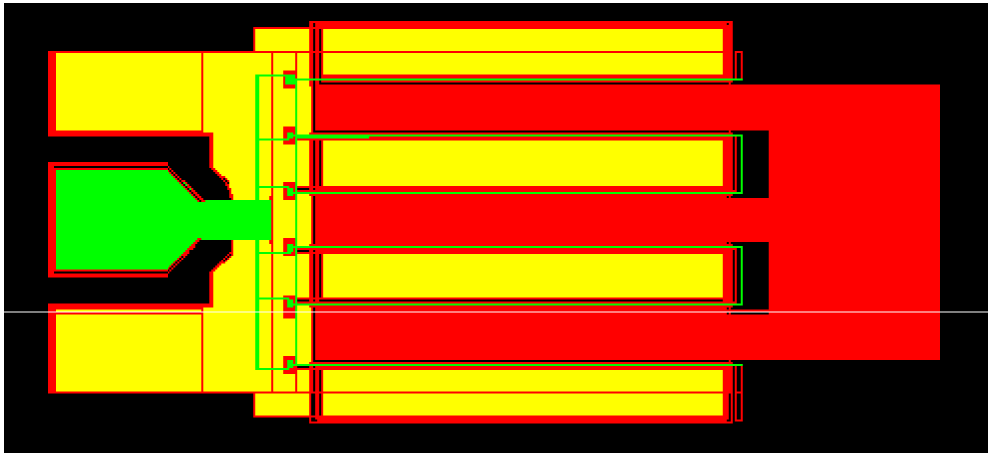


GaN Systems

Need to evaluate reliability

Parameter	CoolMOS	Si IGBT	GaN Cascode	GaN E-HEMT
Rating (V/I)	700/28	600/60	600/17	650/30
R_{ON} (mΩ)	70	40	150	52
Q_G (nC)	64	165	6.2	6.5
E_{SW} (µJ)	2300	1380	500	150
T_{jmax} (°C)	150	150	150	150
Need External Body Diode?	Yes	Yes	Yes	No Bidirectional

GaN HEMT Chip Layout

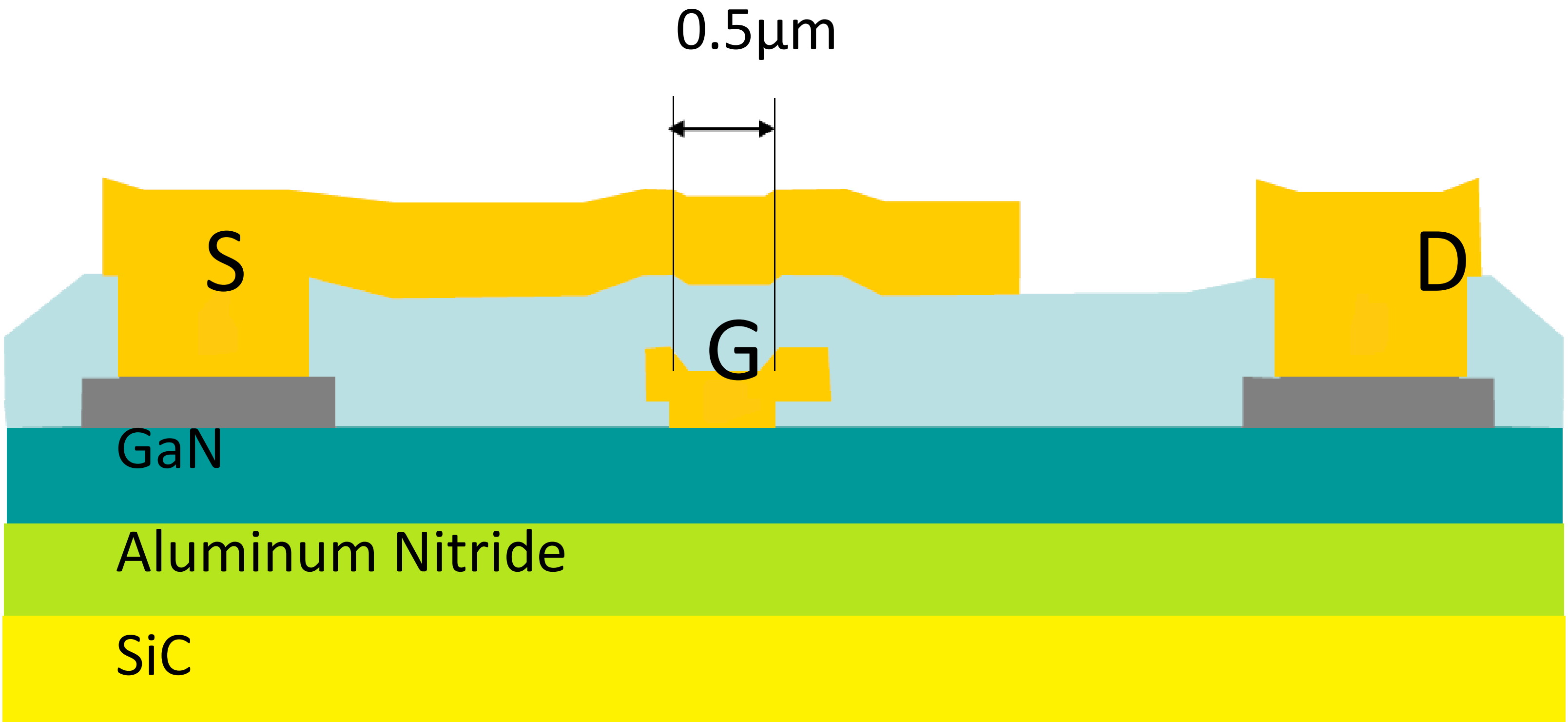


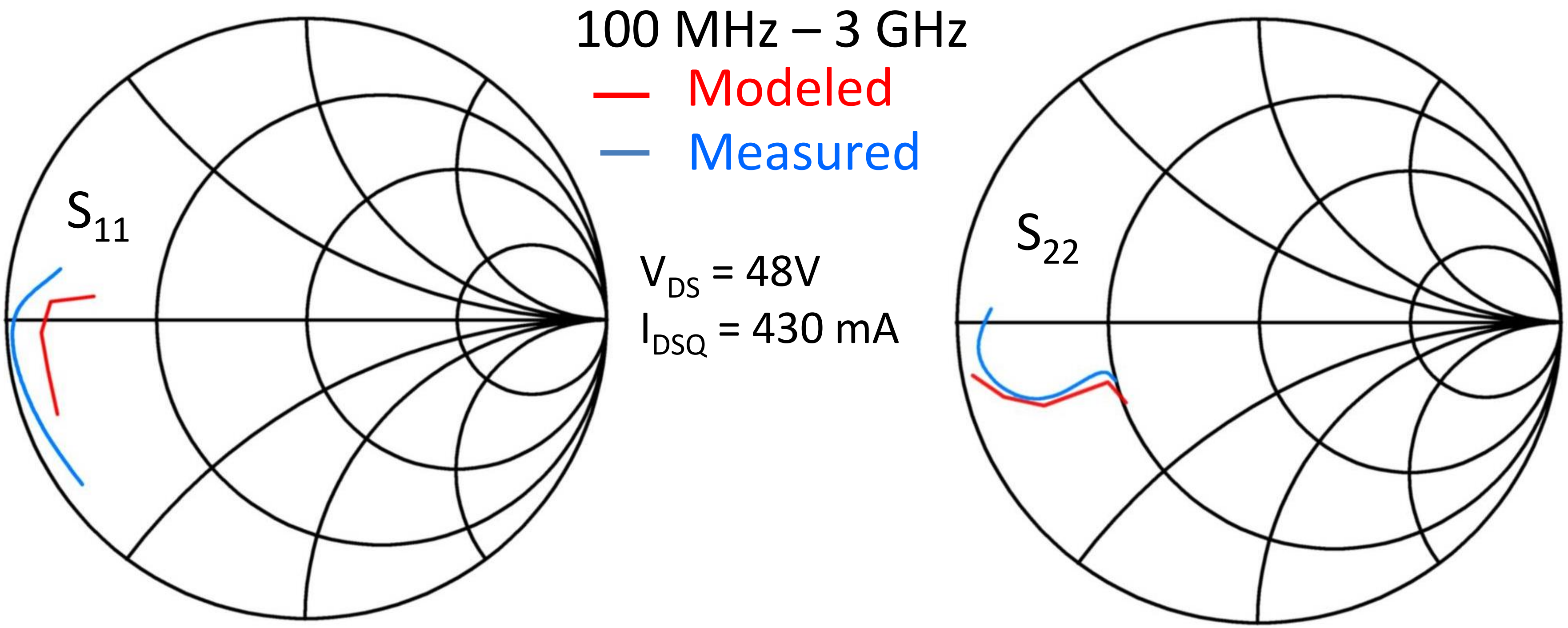
Gate Length = 0.5 µm

Finger Length = 370 µm

Device Width = 22 mm

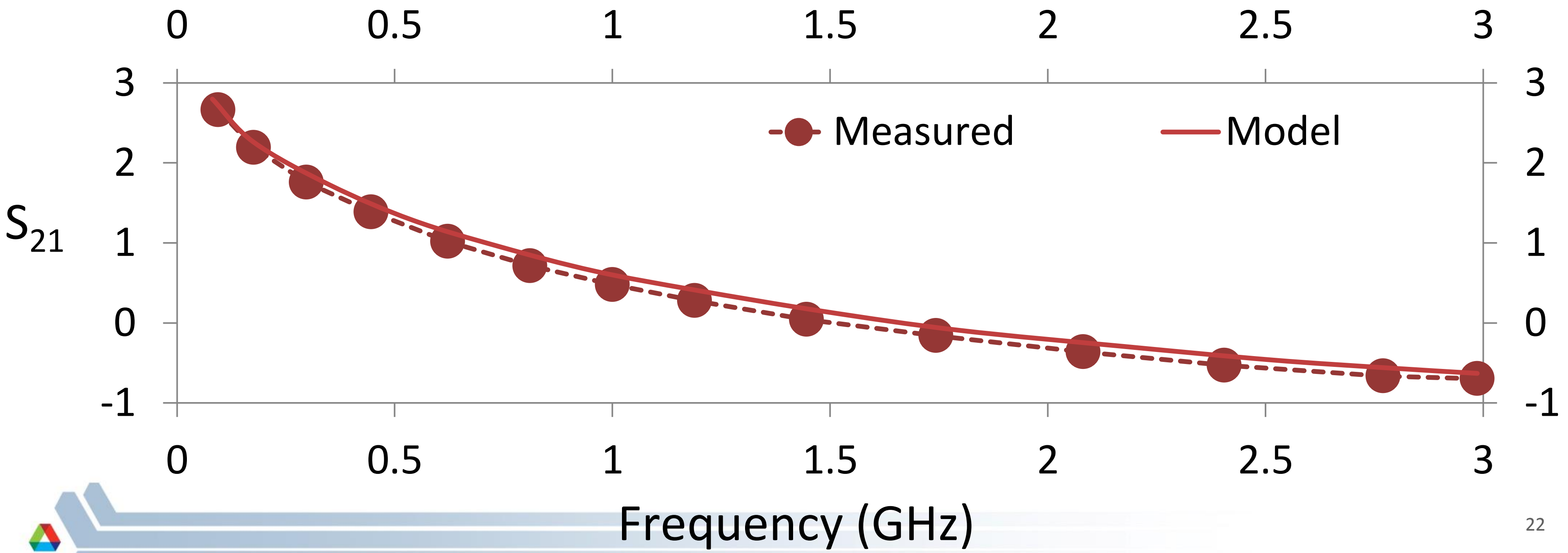
Die Thickness = 4 mils



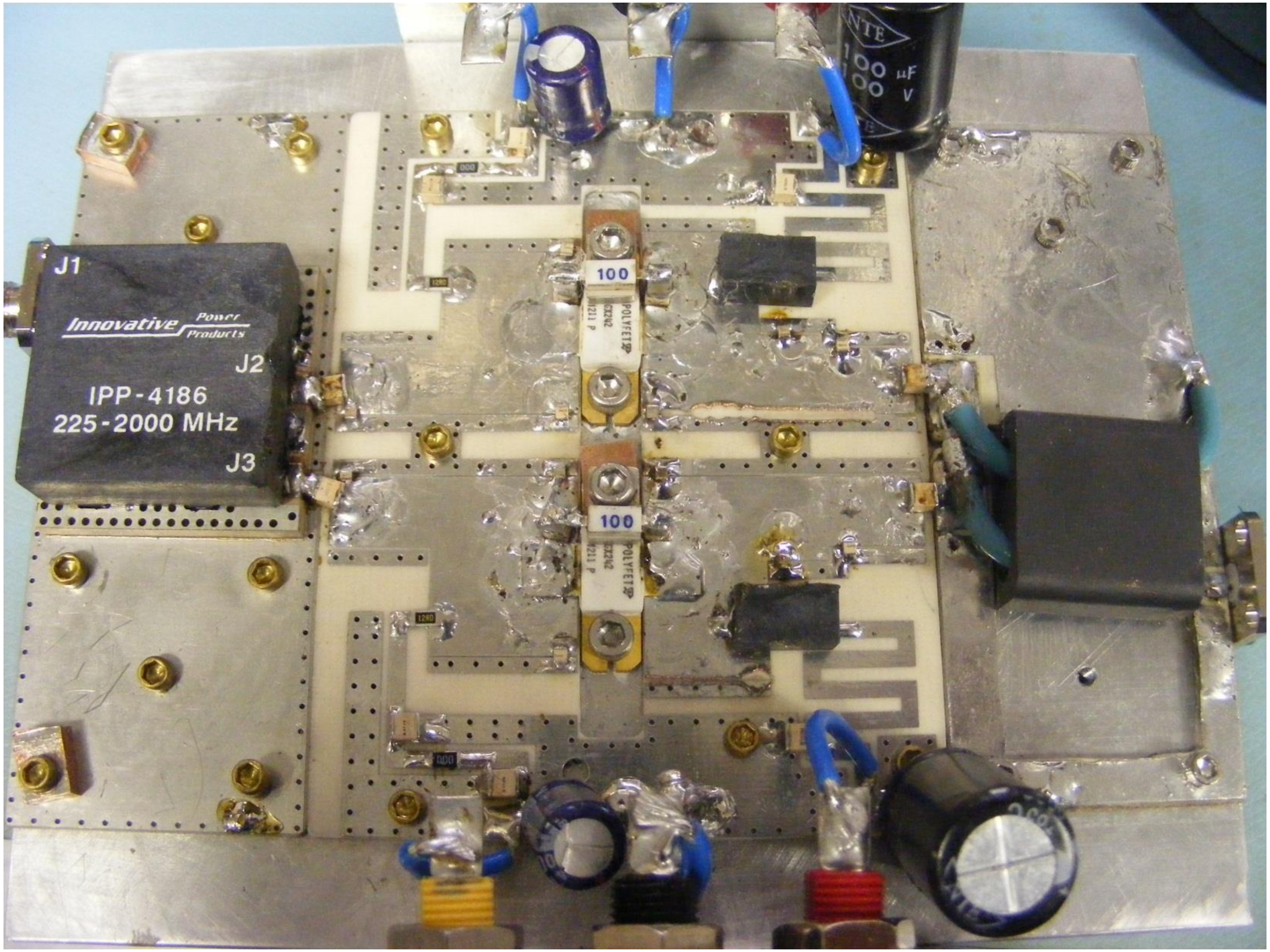


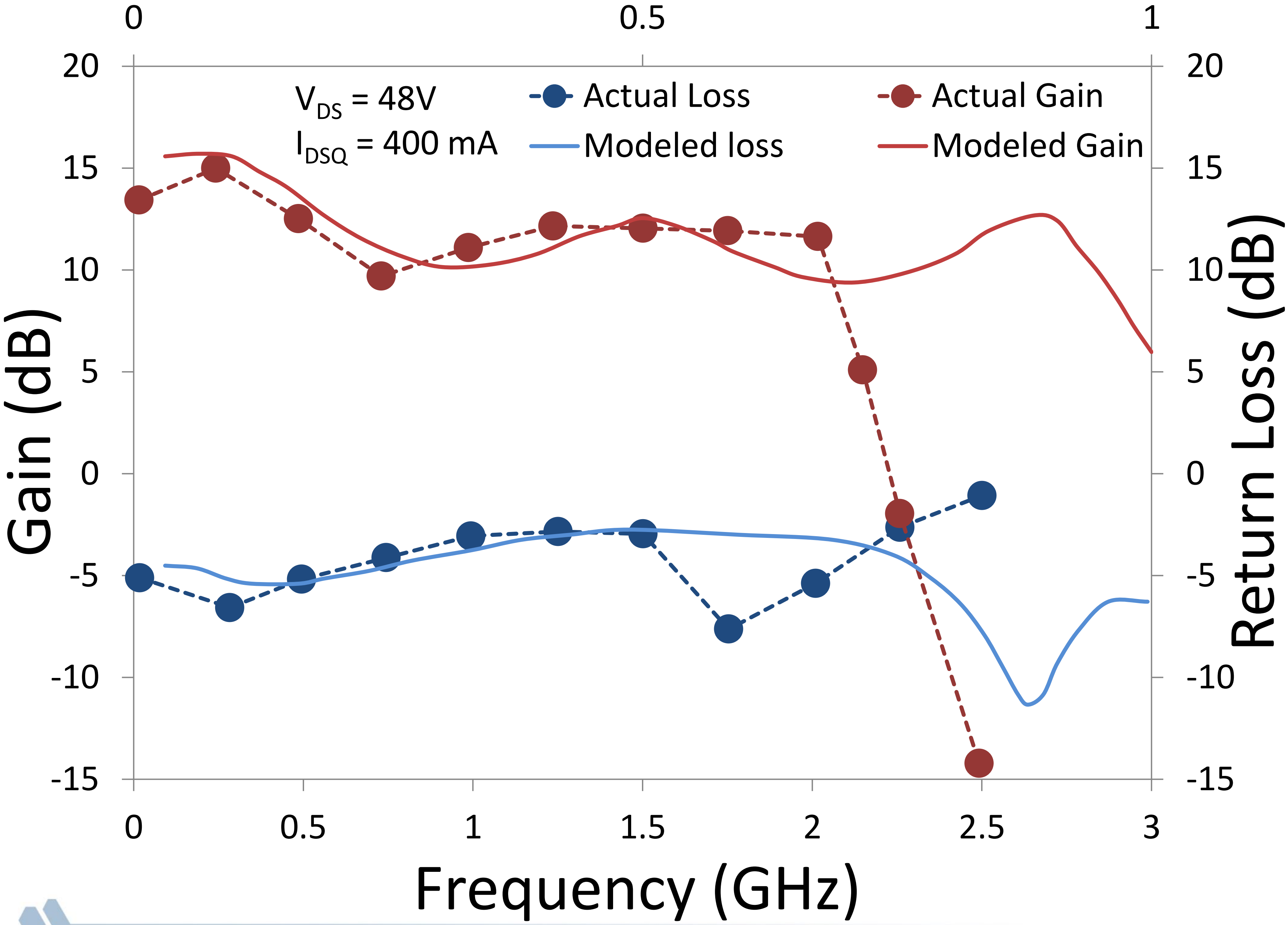
100 MHz – 3 GHz

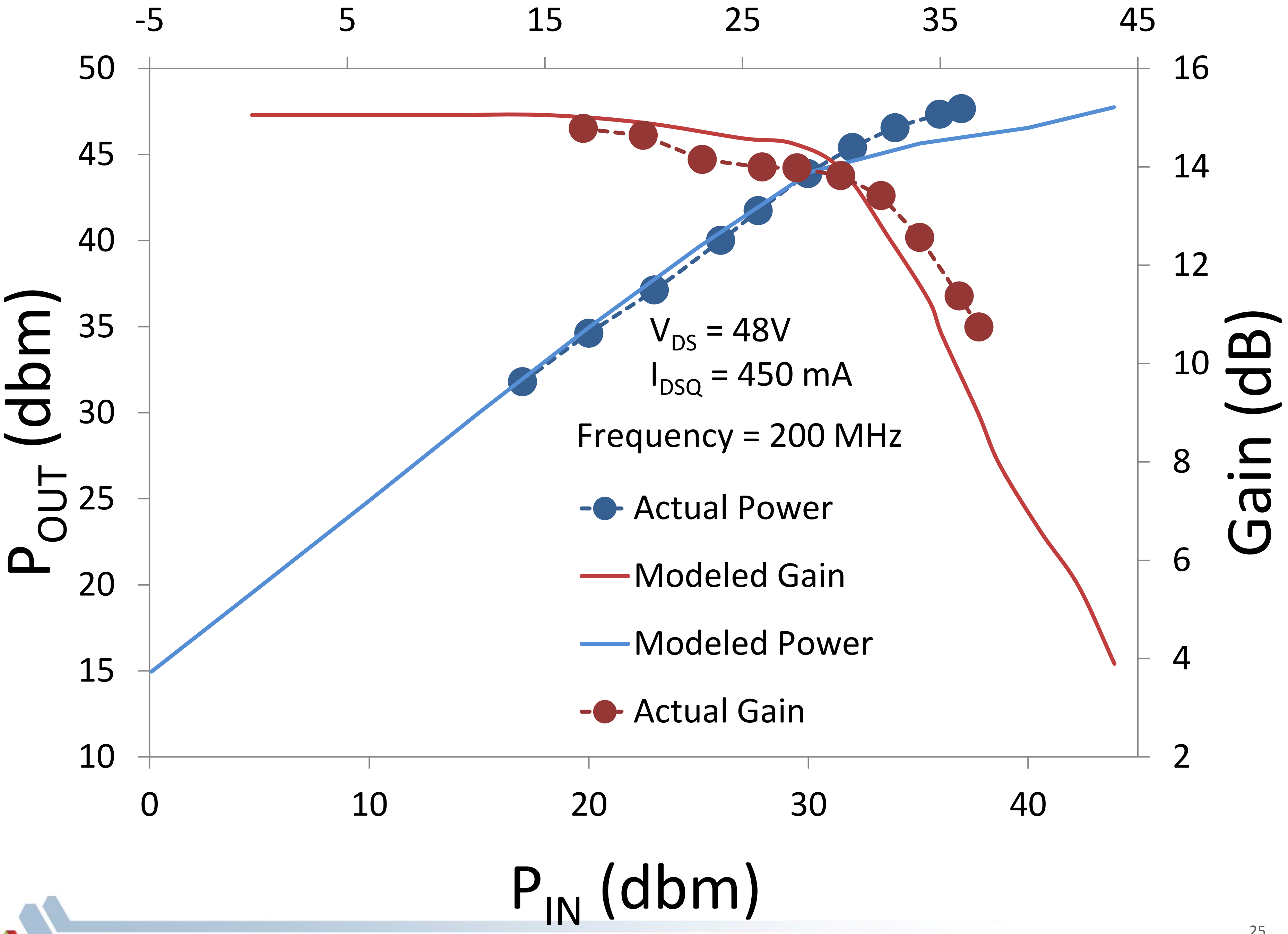
V_{DS} = 48V
I_{DSQ} = 430 mA



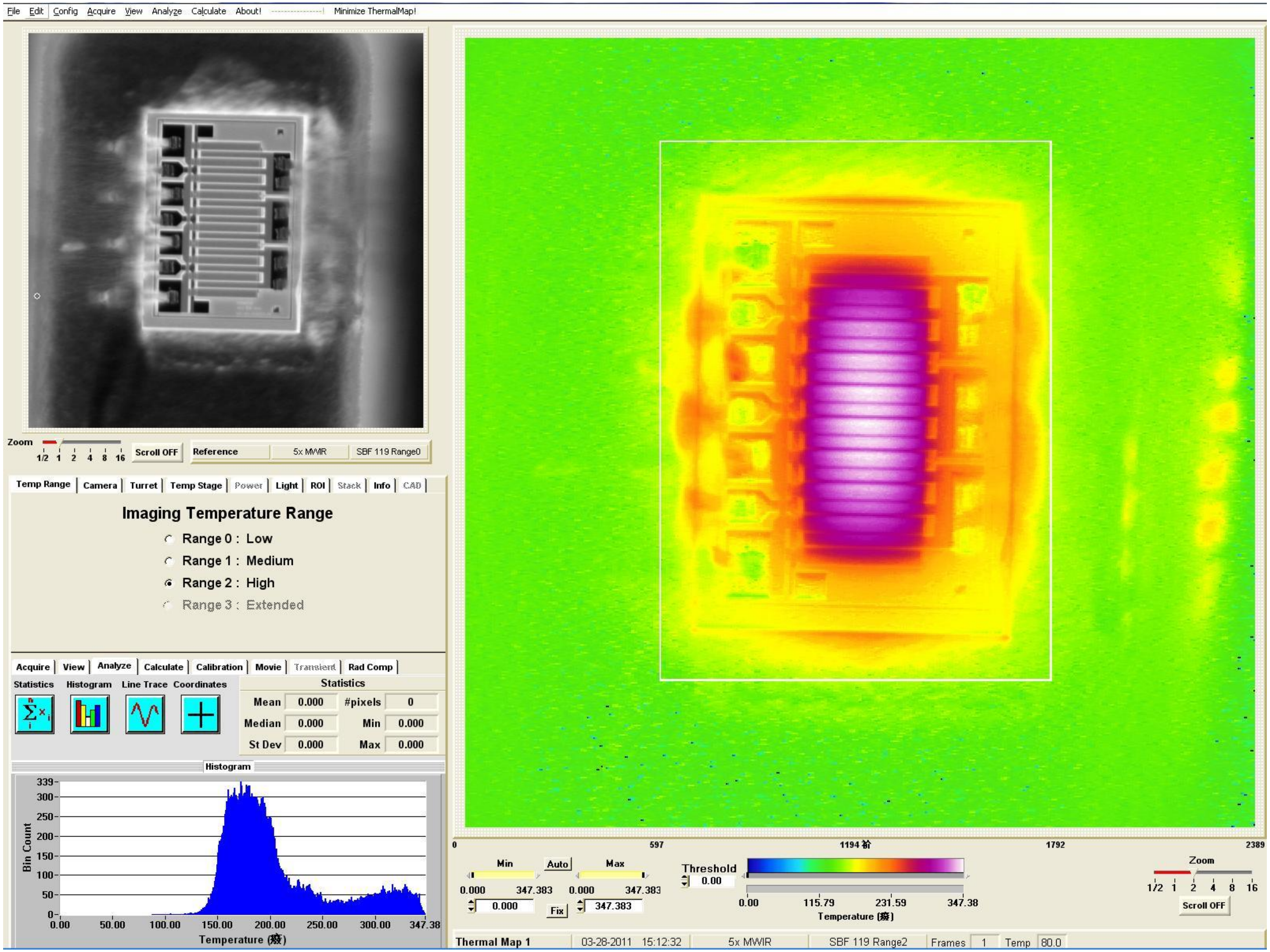
Two Stages Combined – Each Stage Terminates in 25 Ohms




0
0.5
1
20
15
10
5
0
-5
-10
-15
V_{DS} = 48V
I_{DSQ} = 400 mA
Actual Loss
Modeled loss
Actual Gain
Modeled Gain
Gain (dB)
Return Loss (dB)
0
0.5
1
1.5
2
2.5
3
Frequency (GHz)


-5
5
15
25
35
45
50
45
40
35
30
25
20
15
10
16
14
12
10
8
6
4
2
P_{OUT} (dbm)
Gain (dB)
V_{DS} = 48V
I_{DSQ} = 450 mA
Frequency = 200 MHz
Actual Power
Modeled Gain
Modeled Power
Actual Gain
0
10
20
30
40
P_{IN} (dbm)

Thermal Effects



Imaging Temperature Range

○ Range 0 : Low
○ Range 1 : Medium
● Range 2 : High
○ Range 3 : Extended

Statistics

Mean	0.000	#pixels	0
Median	0.000	Min	0.000
St Dev	0.000	Max	0.000

Min: 0.000 347.383 — 0.000

Max: 0.000 347.383 — 347.383

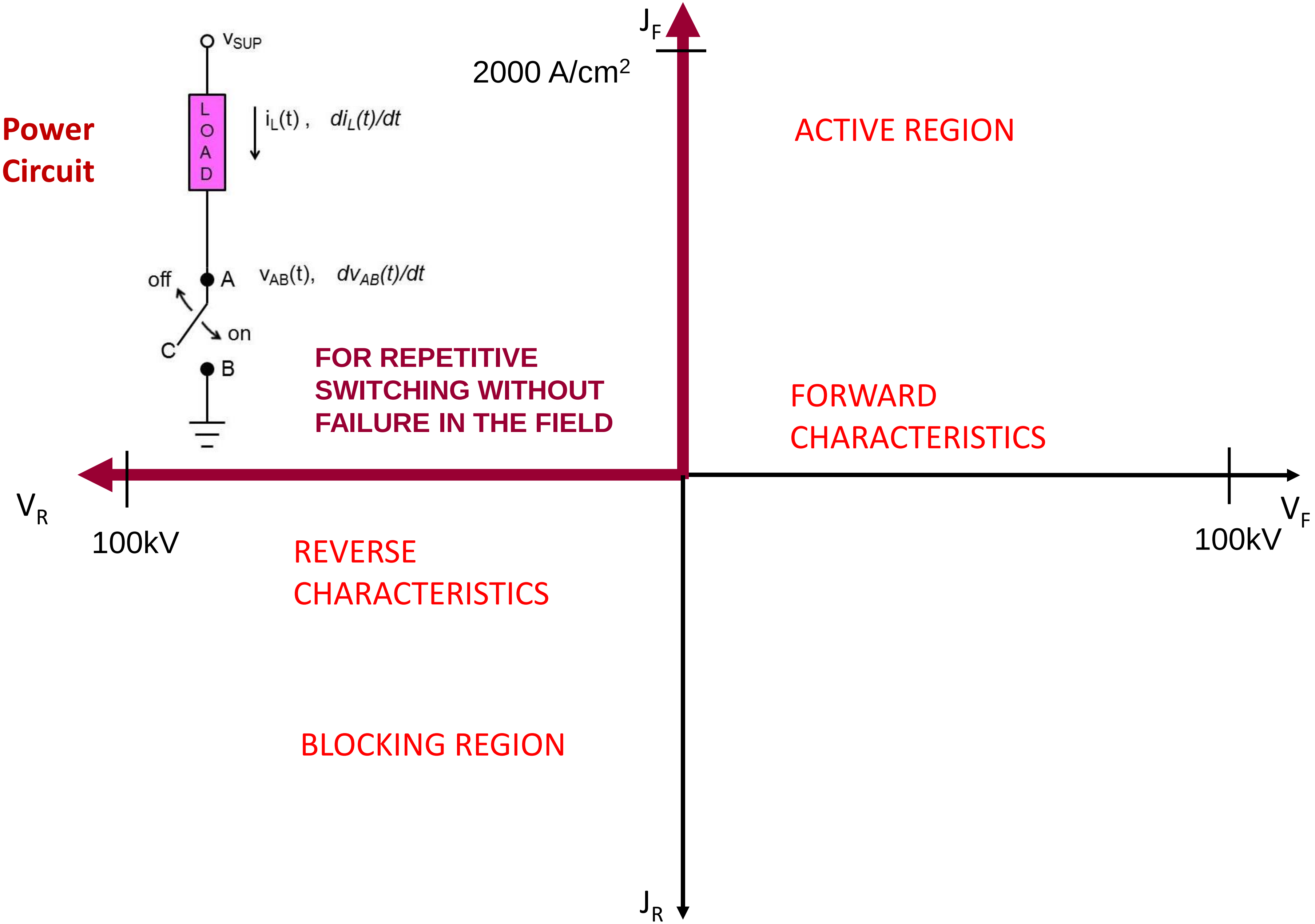
Threshold: 0.00

Thermal Map 1 | 03-28-2011 15:12:32 | 5x MWIR | SBF 119 Range2 | Frames 1 | Temp 80.0

The Search for the Ideal Semiconductor Power Switch

(dates back to the 1950's)

Power Circuit



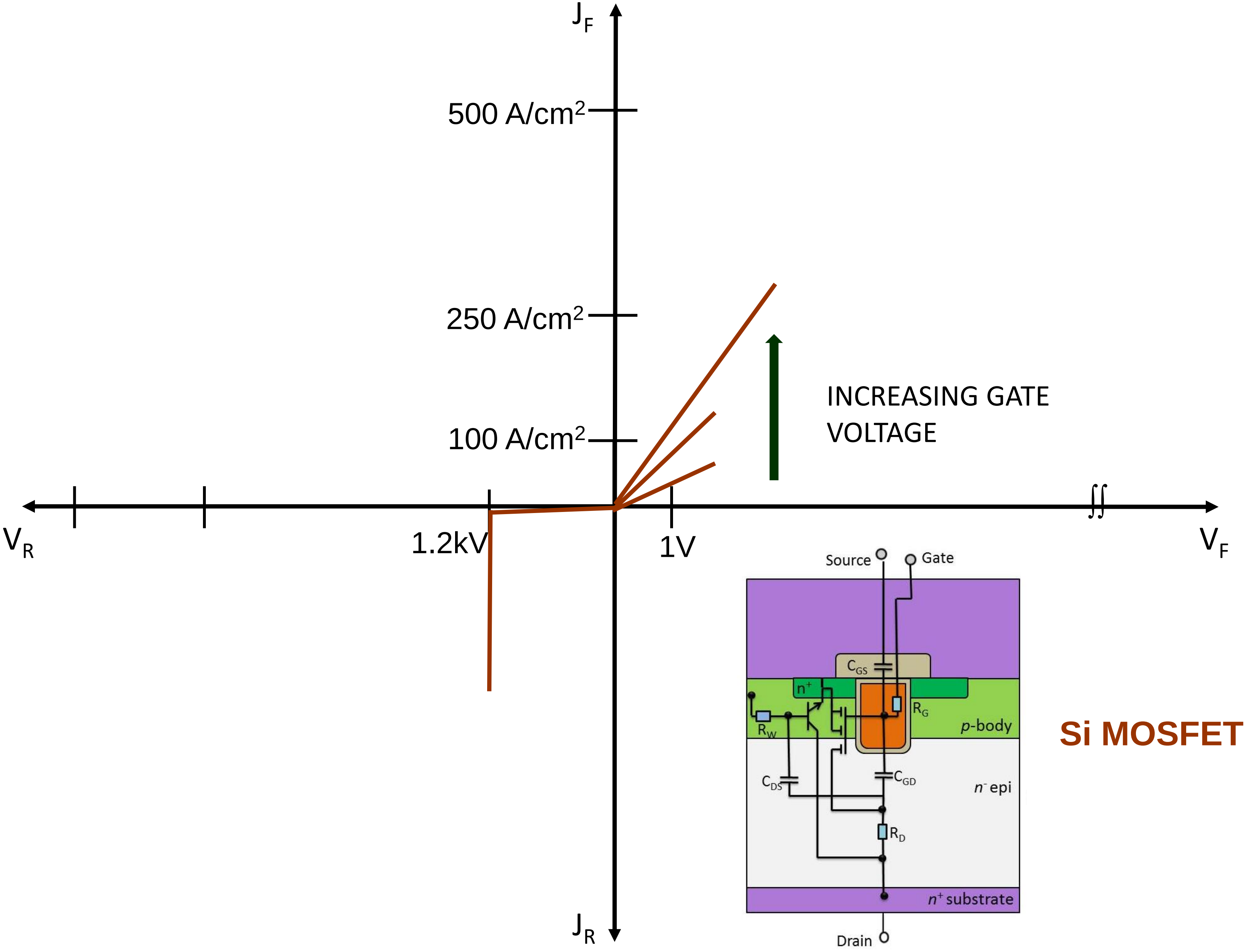
FOR REPETITIVE SWITCHING WITHOUT FAILURE IN THE FIELD

ACTIVE REGION

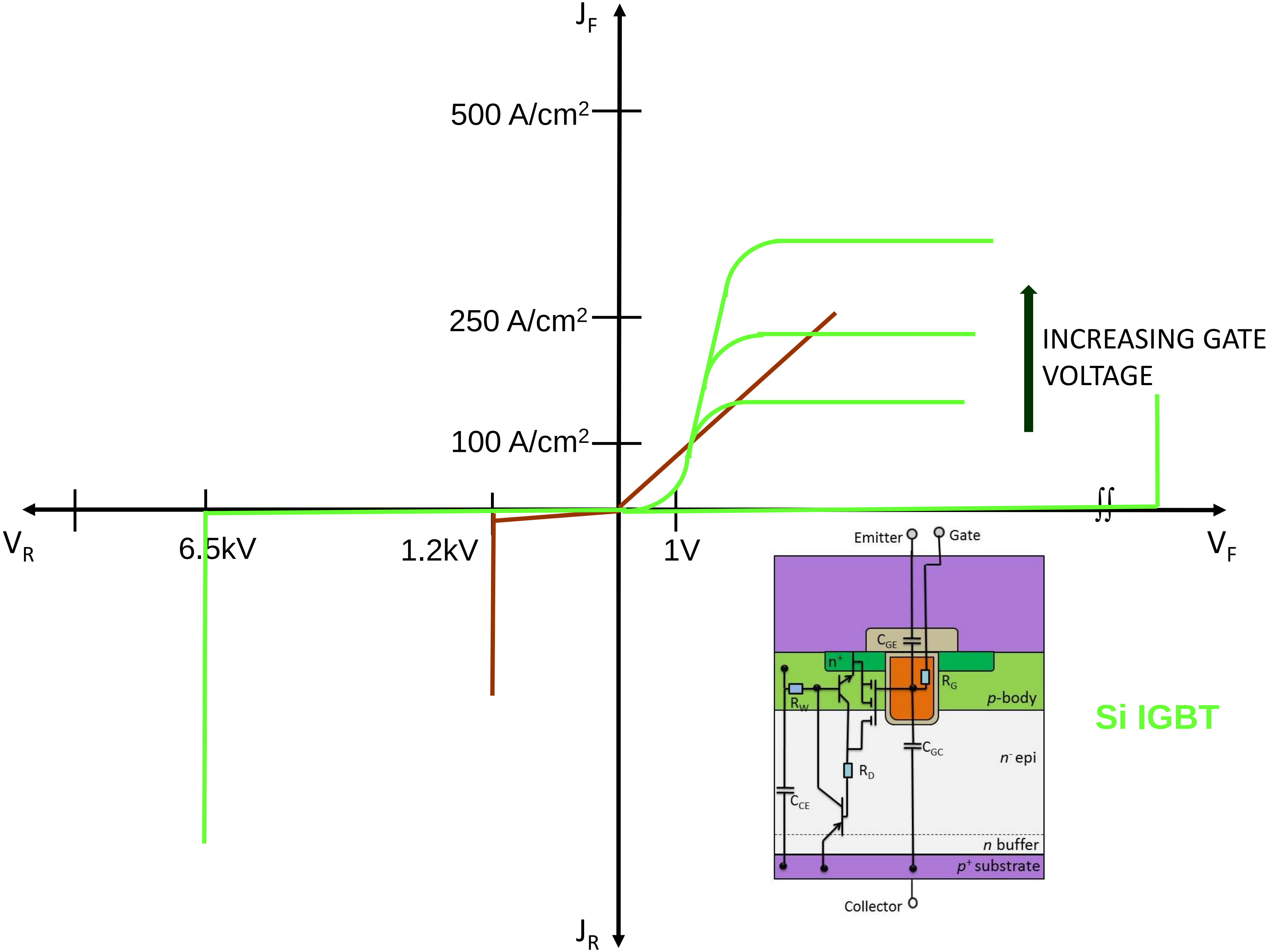
FORWARD CHARACTERISTICS

REVERSE CHARACTERISTICS

BLOCKING REGION

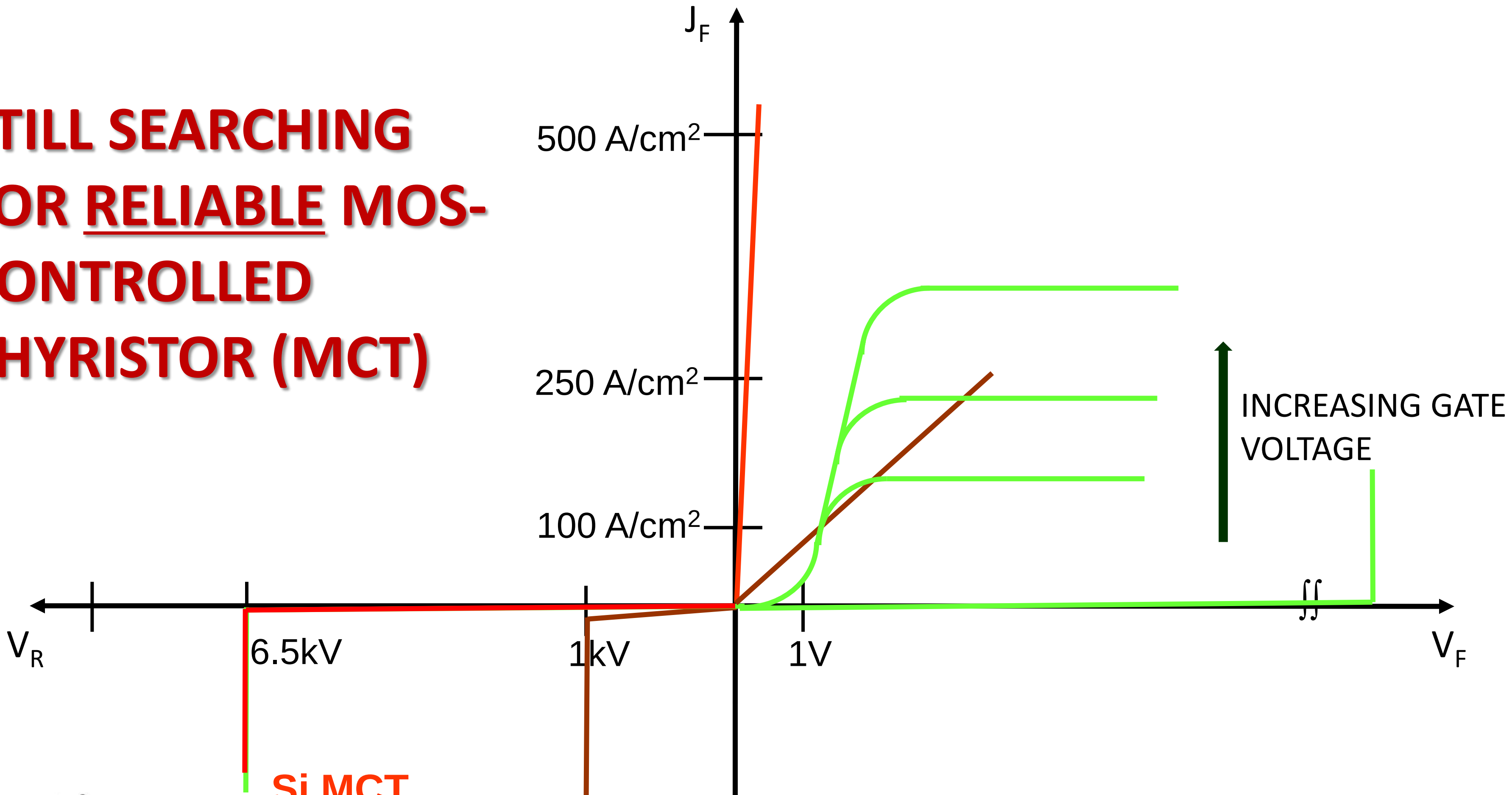

J_F
500 A/cm²
250 A/cm²
100 A/cm²
INCREASING GATE VOLTAGE
V_R
1.2kV
1V
V_F
J_R
Source
Gate
C_GS
n+
R_G
R_W
p-body
C_DS
C_GD
n- epi
R_D
n+ substrate
Drain

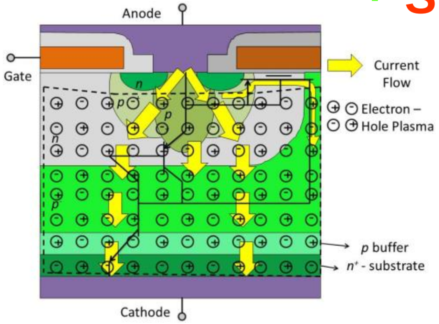
Si MOSFET


J_F
500 A/cm^2
250 A/cm^2
100 A/cm^2
INCREASING GATE VOLTAGE
V_R
6.5kV
1.2kV
1V
V_F
J_R
Emitter
Gate
C_{GE}
n^+
R_G
R_W
p-body
C_{GC}
n$^-$ epi
R_D
C_{CE}
n buffer
p^+ substrate
Collector

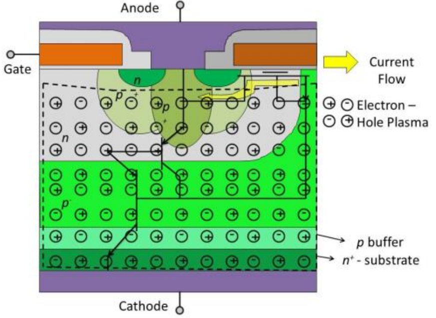
Si IGBT

STILL SEARCHING FOR RELIABLE MOS-CONTROLLED THYRISTOR (MCT)



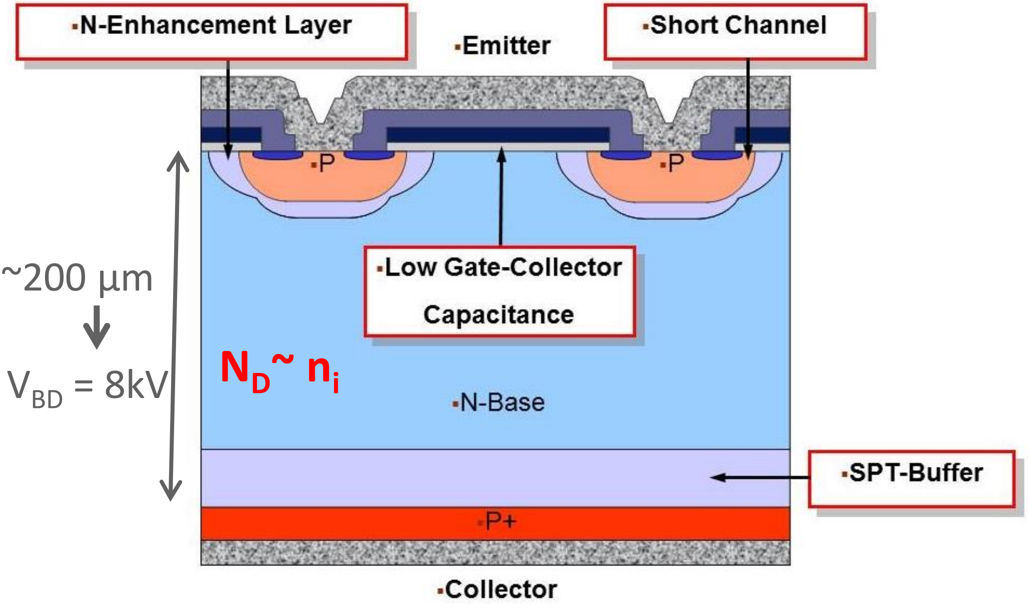


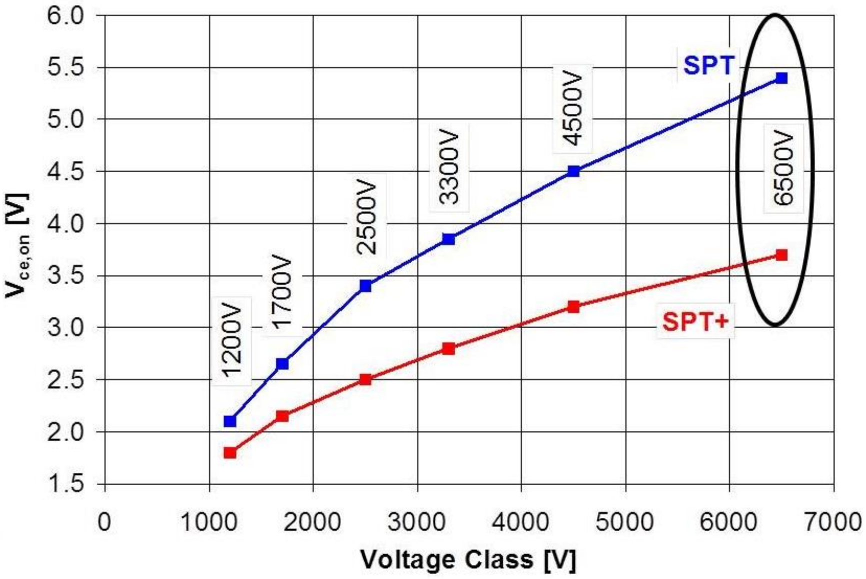
Turn-on



Turn-off **FAILURE**

K. Shenai, *JCSC* (2013)





6500V SPT+ HiPak Modules
Rated at 750A

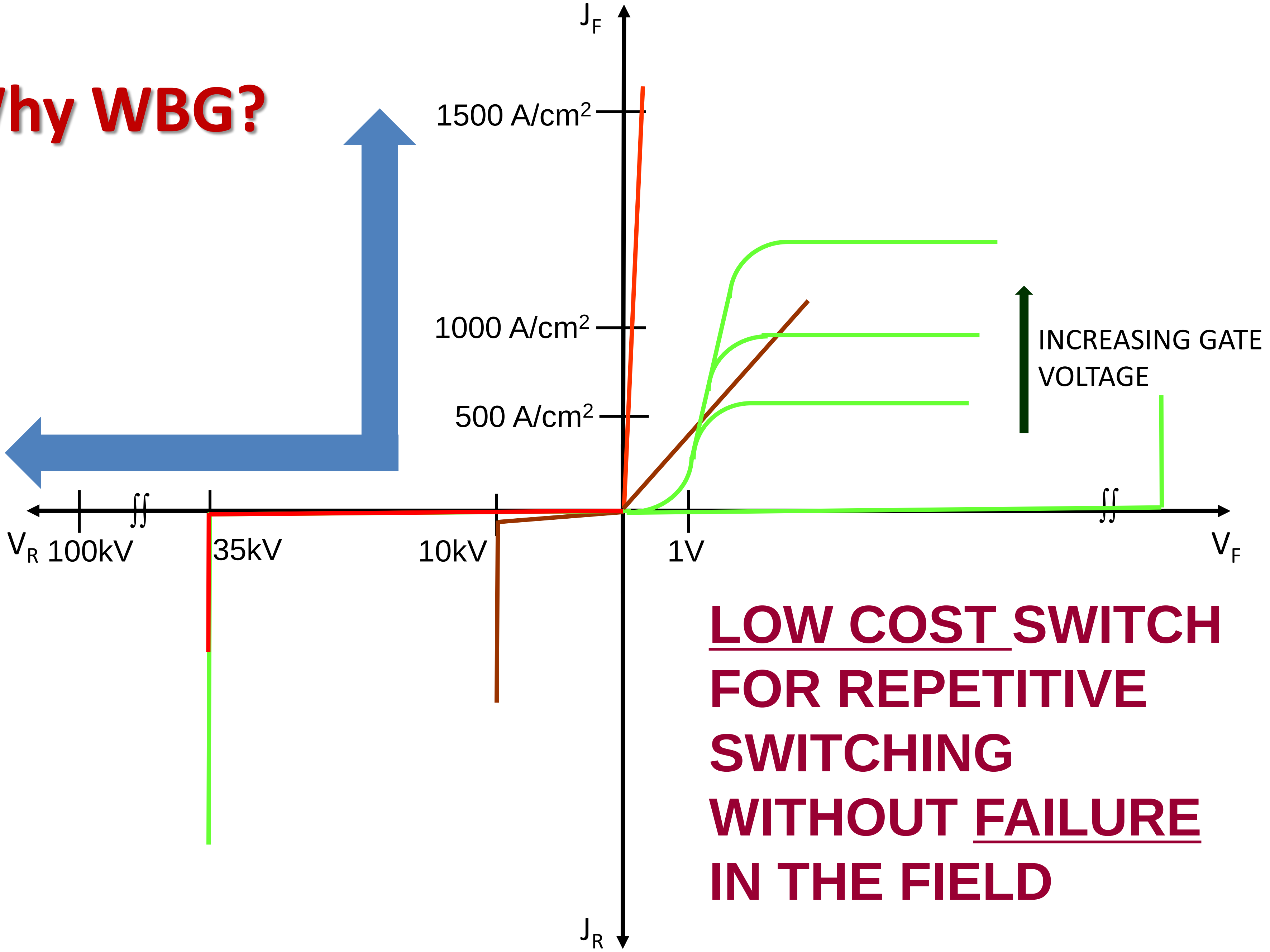
Need <u>single-chip</u> WBG MOSFETs with:

$V_{on} < 1V$
$I_{on} > 200A$
$T_{jmax} > 200°\ C$

at the same <u>cost</u> and with same <u>reliability</u> as silicon IGBT

K. Shenai, *IEEE PELS Magazine, pp. 27-32, Sept. 2014*

Why WBG?

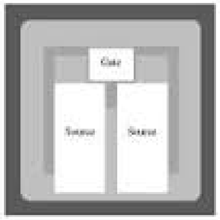


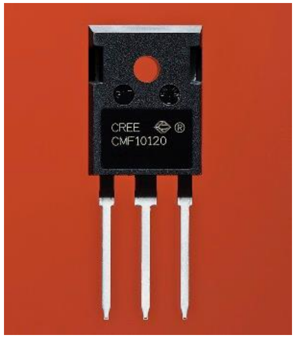
LOW COST SWITCH FOR REPETITIVE SWITCHING WITHOUT FAILURE IN THE FIELD

K. Shenai *et al,* "Optimum Semiconductors for High-Power Electronics," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1811-1823, September 1989.

Key Challenges and Opportunities

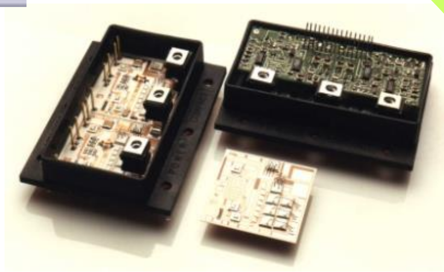
- High chip and module costs

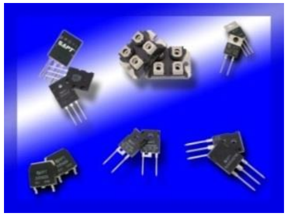




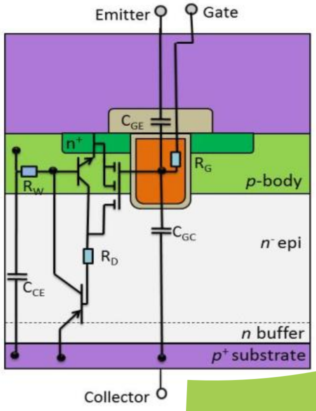
- Non-optimal performance
- Long-term reliability in a power converter unknown

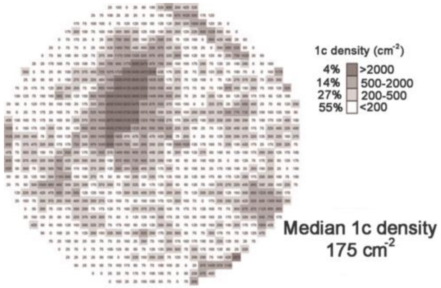
Fragmented Industry Supply Chain



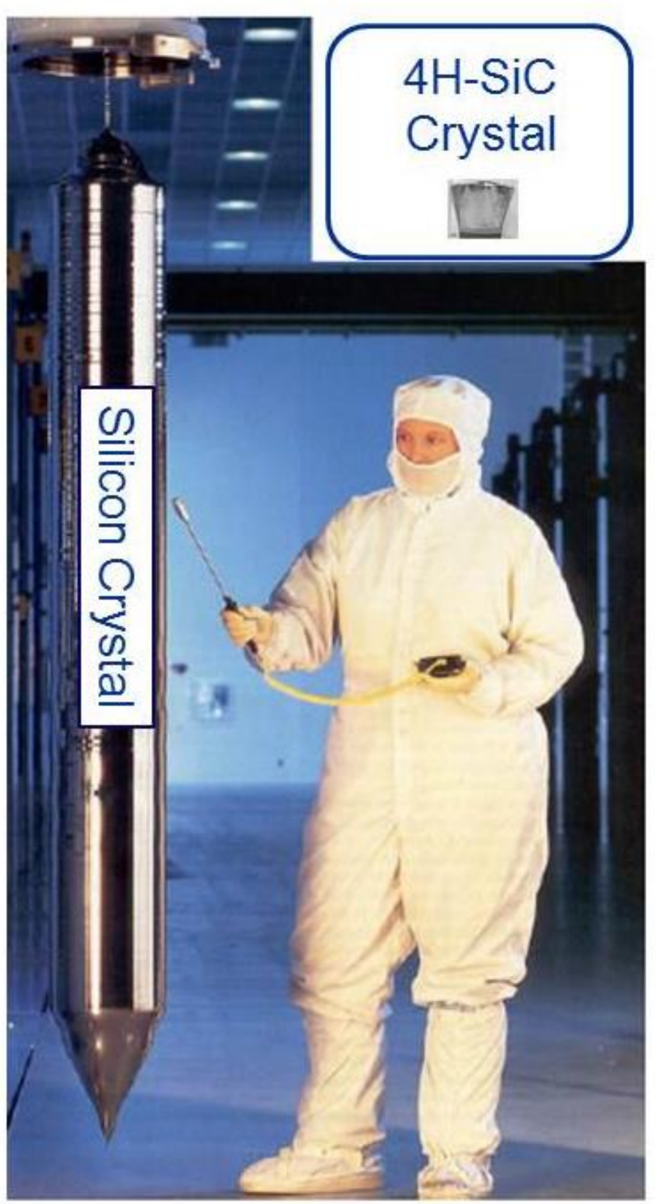


- **High cost**
- **Unknown reliability**

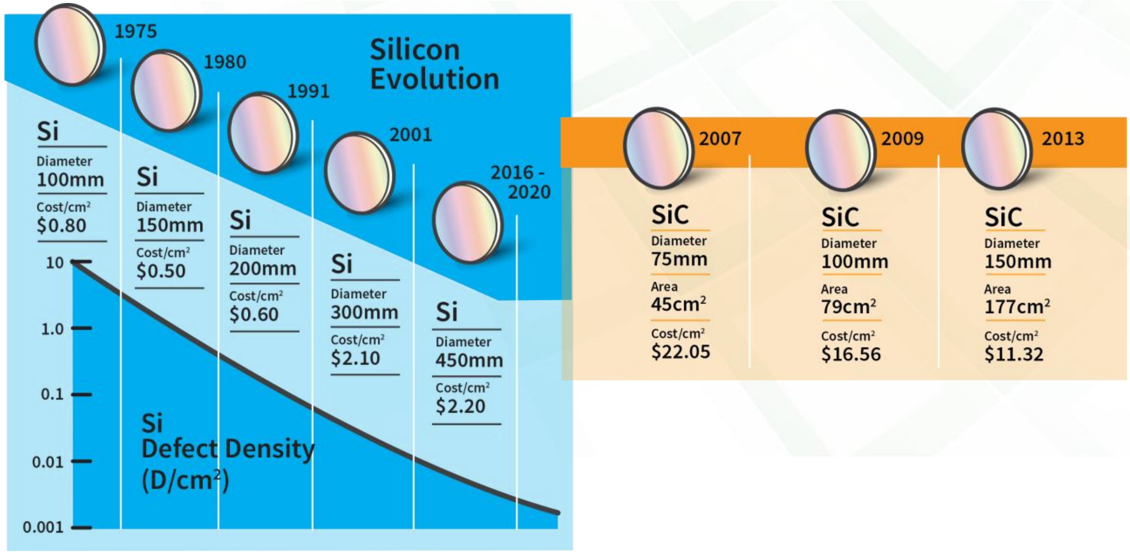




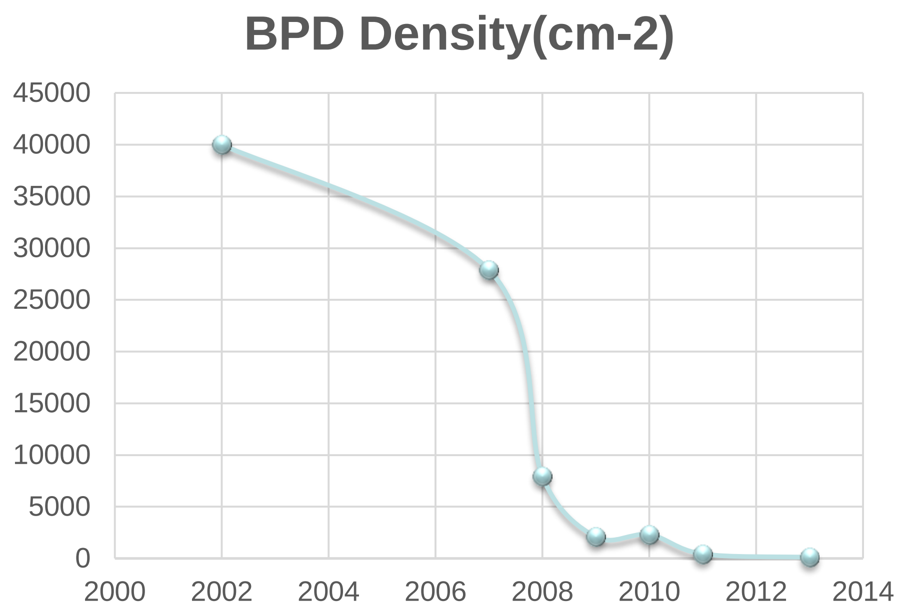
Expensive and Defective Wafers

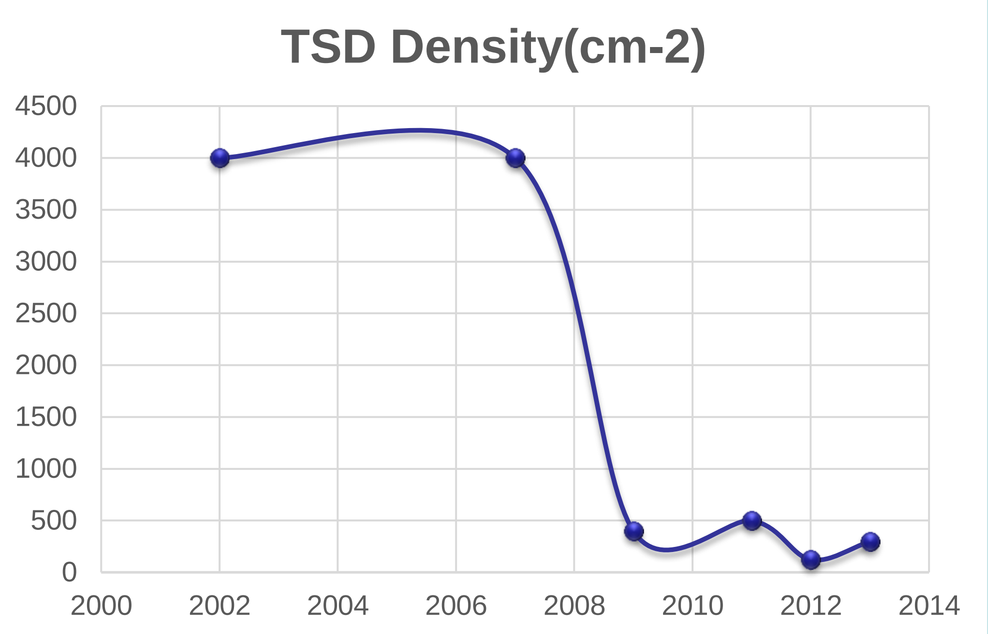


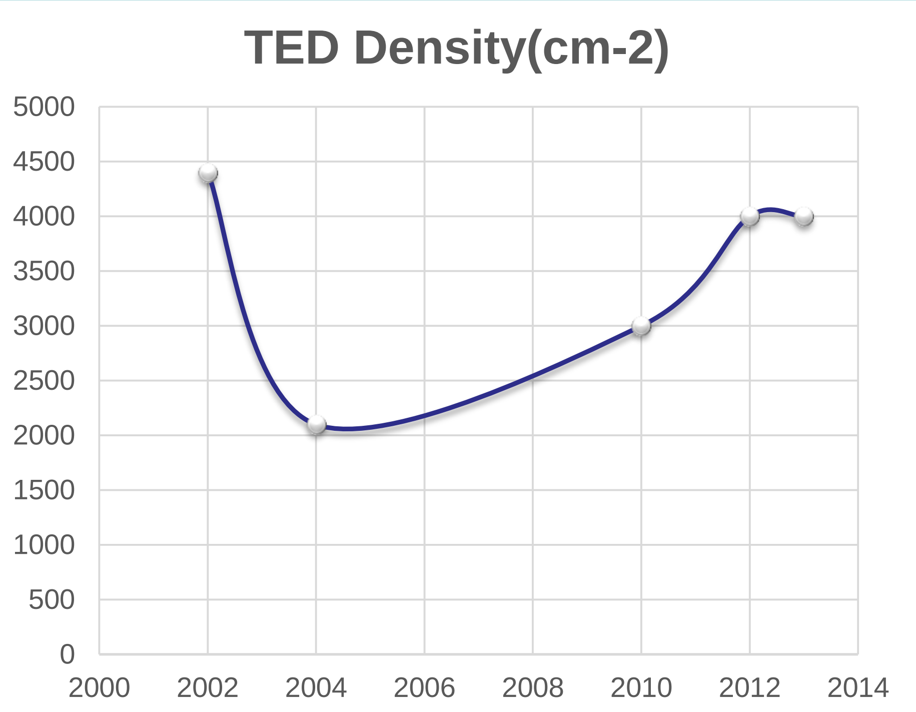
Parameter	Silicon	SiC
Growth Temperature	< 1000°C	> 2000°C
Method	Czochralski	PVT
Defect Density	< 1/cm²	$10^2 – 10^4$ cm^{-2}
Cost	Low	> 20X

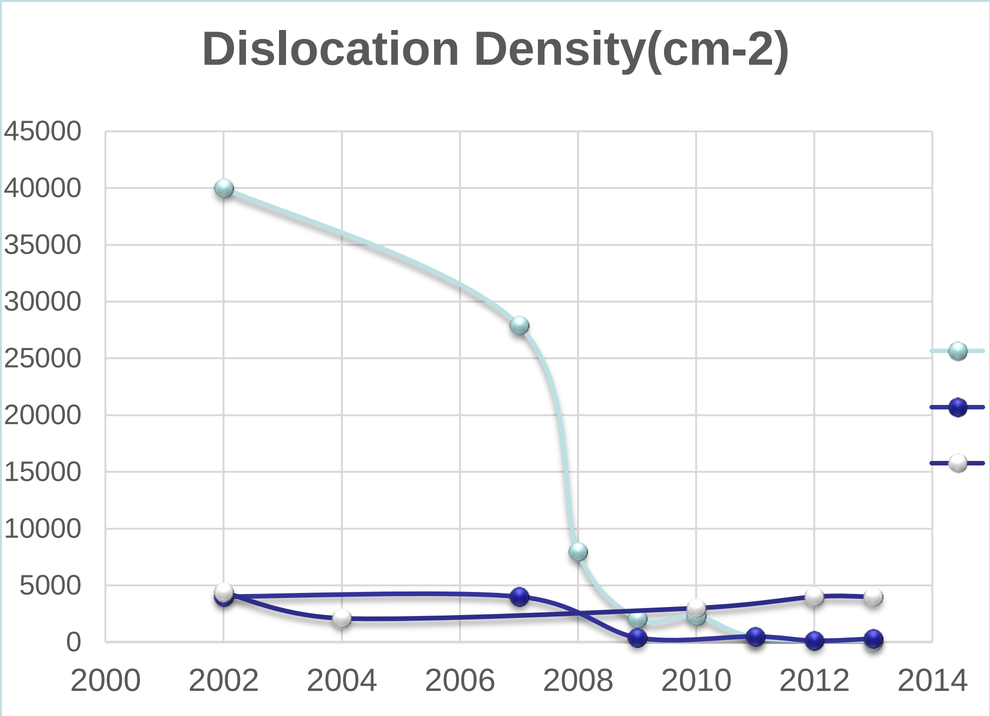


Substrate Dislocation Density Trends (collaborator: Dr. Mike Dudley, SUNY-SB)


BPD Density(cm-2)

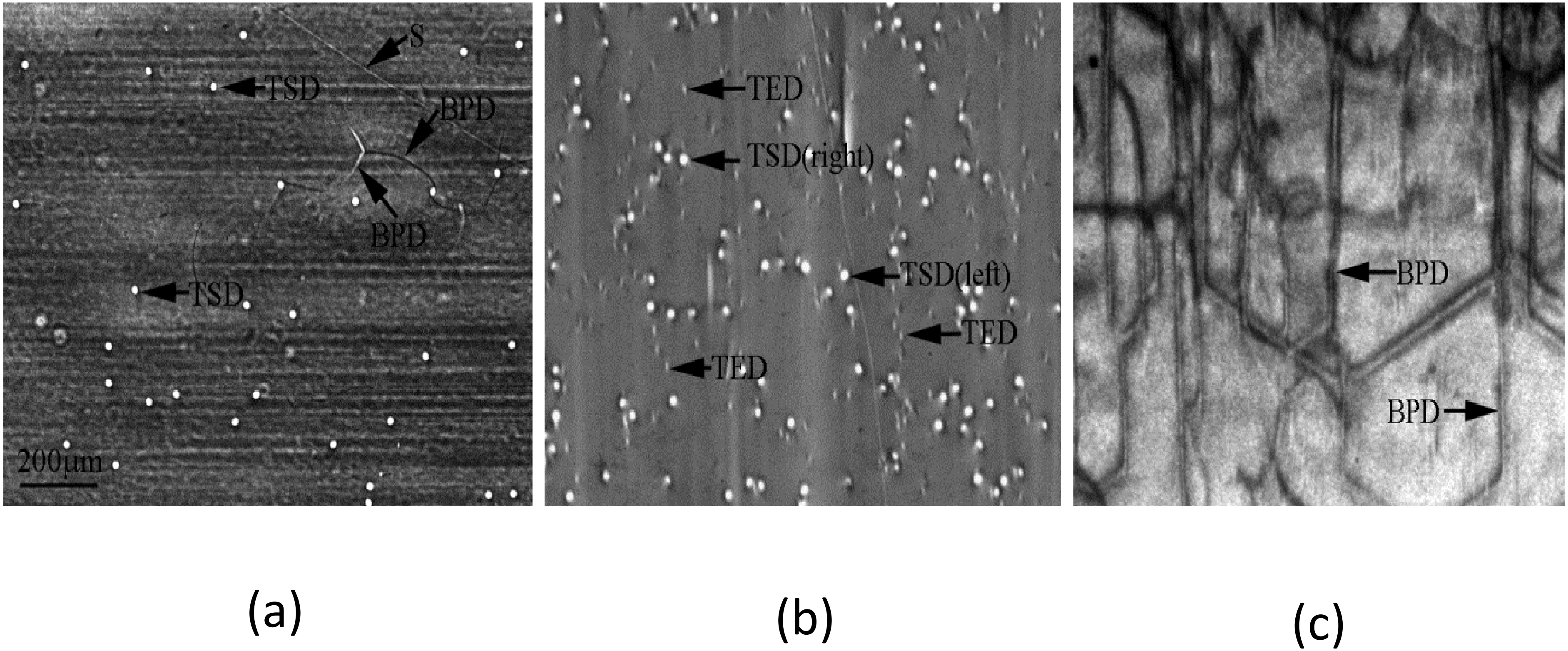

TSD Density(cm-2)


TED Density(cm-2)


Dislocation Density(cm-2)

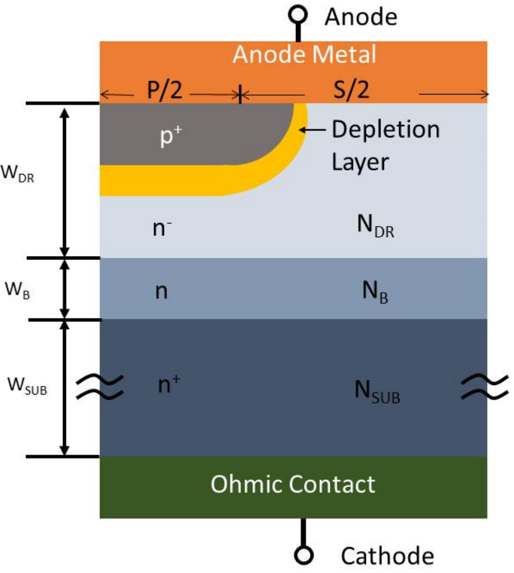
Defects in State-of-the-Art Commercial 4H-SiC Wafers

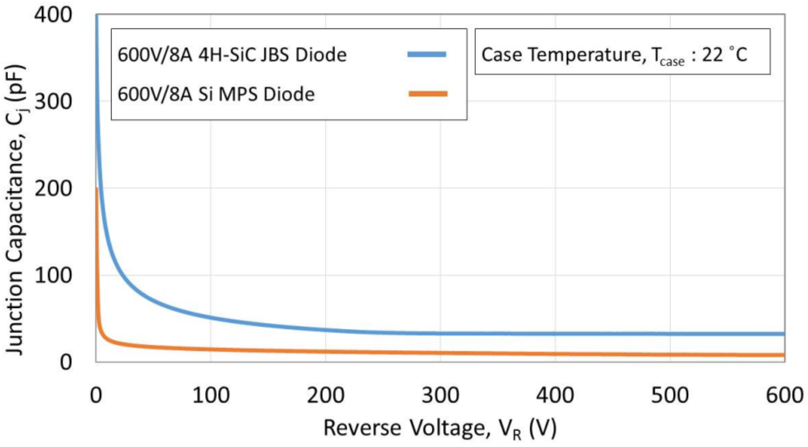
(collaborator: Dr. Mike Dudley, SUNY-SB)

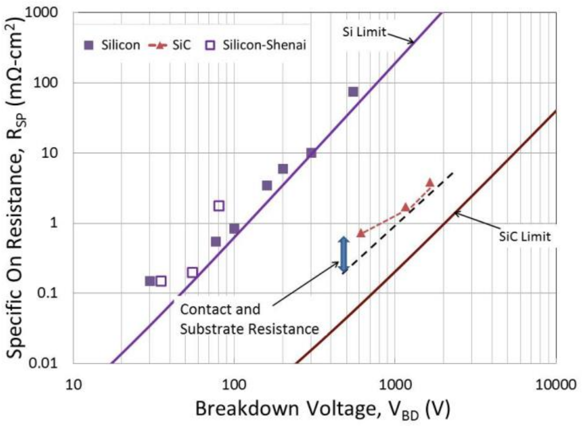


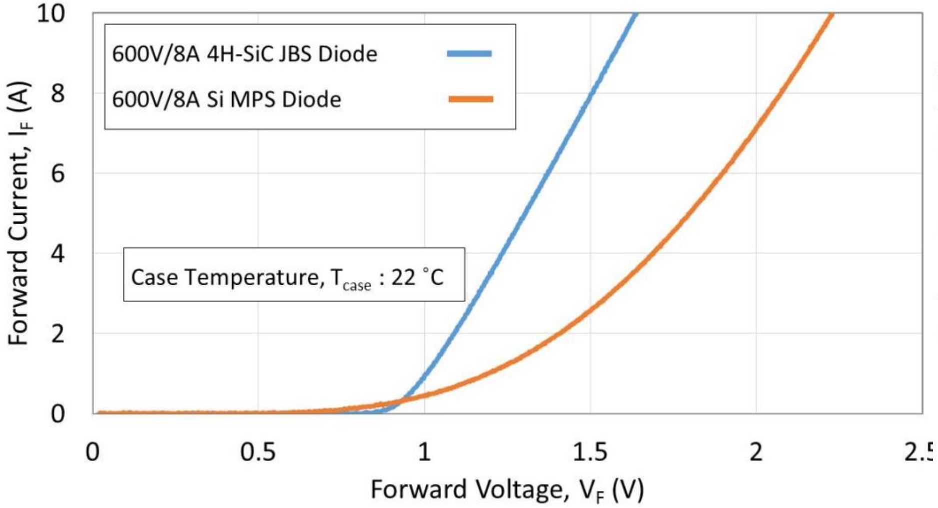
High resolution synchrotron monochromatic X-ray topographs recorded at Argonne's Advanced Photon Source (APS) facility. (a) Back-reflection X-ray topograph (g = 0004) images of close-core threading screw dislocations (TSDs) and basal plane dislocations (BPDs) in a (0001) 4H SiC wafer; (b) Grazing incidence X-ray topograph (g = 11-28) of 4H-SiC substrate showing TSDs (right and left handed) and TEDs; (c) Transmission X-ray topograph showing the images of BPDs.

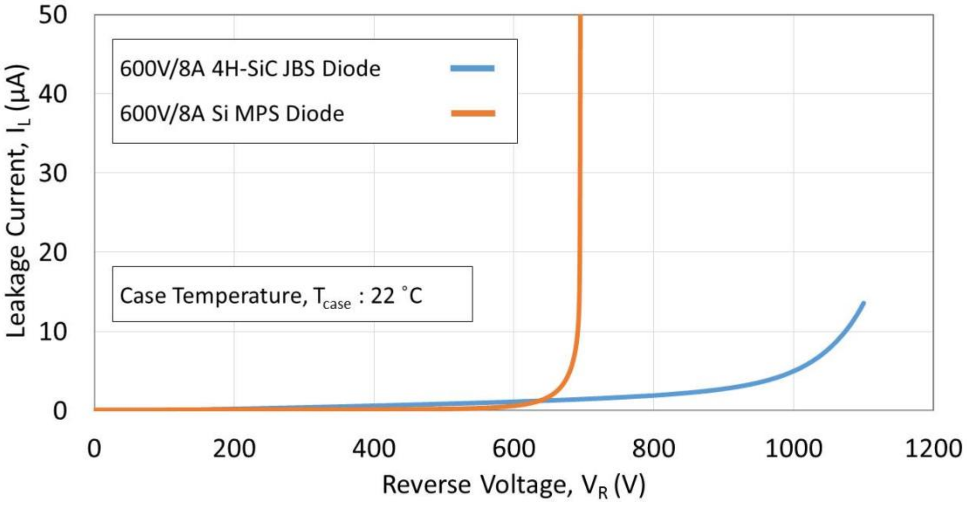
Performance Evaluation of 4H-SiC JBS Power Diode







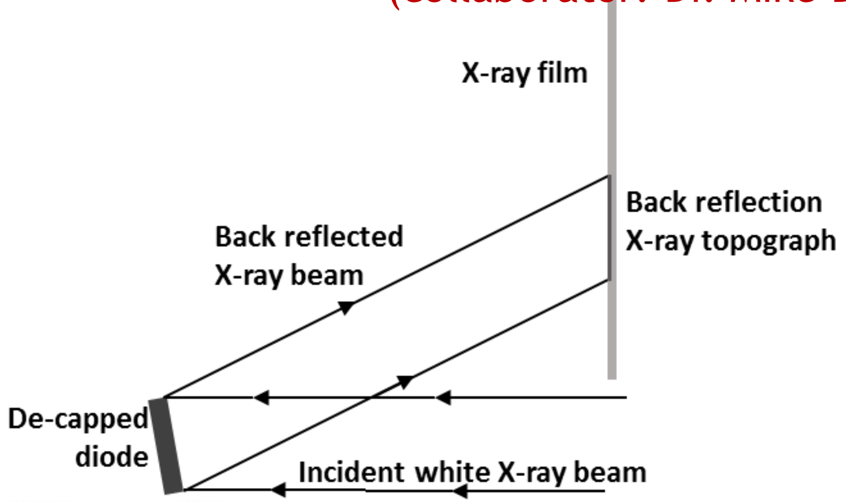


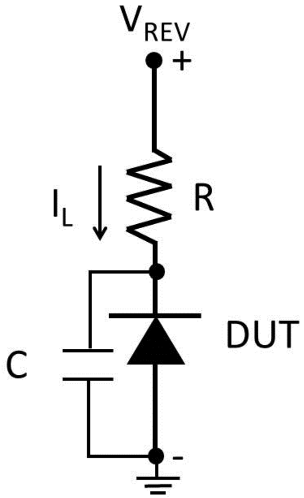


K. Shenai, *IEEE Trans. ED*, Feb. 2015 (to be published)

Defect-Induced Lattice Deformation in 600V SiC JBS Diode

(collaborator: Dr. Mike Dudley, SUNY-SB)





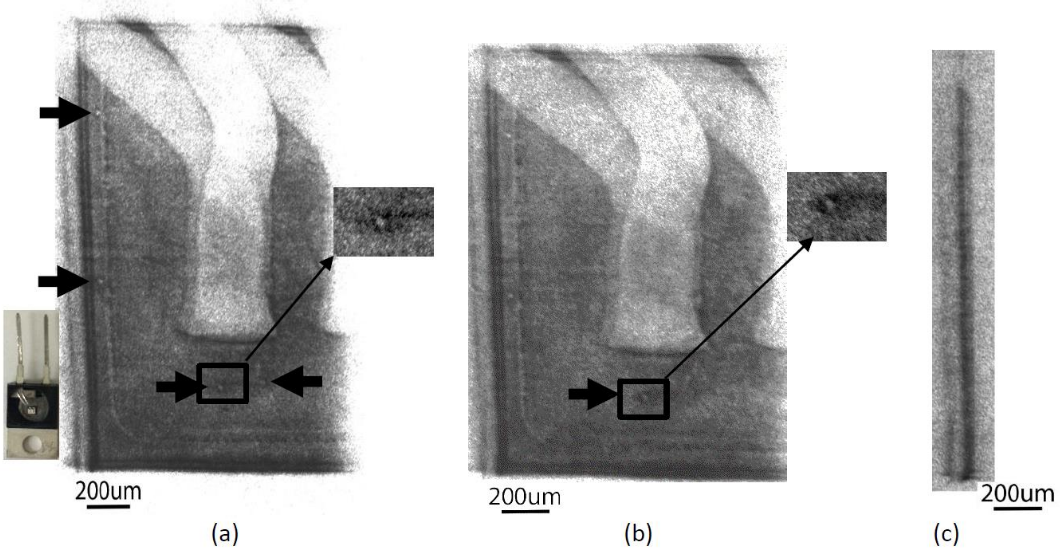


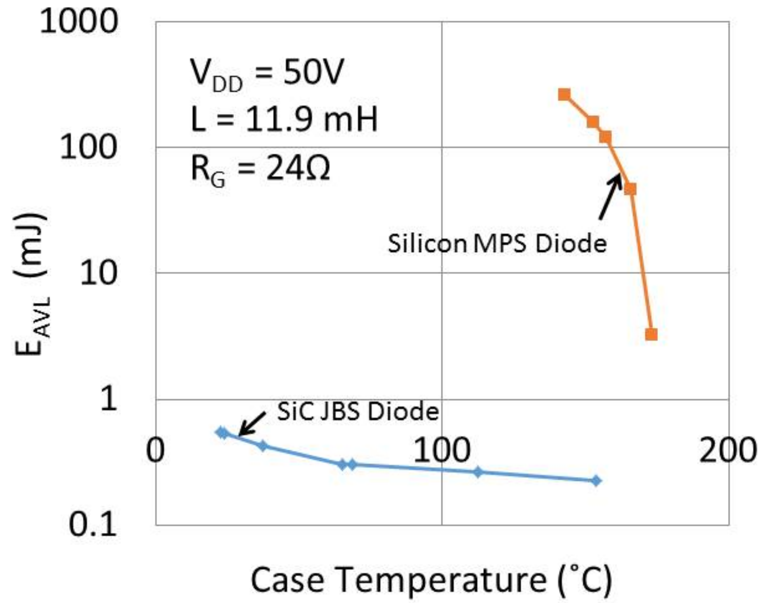
Figure 2. Back reflection topographs recorded from de-capped SiC diode Cree 1AA at (a) 700V showing contrast from TSDs as indicated by arrows; (b) 900V showing enhanced contrast at 1 threading screw dislocation as indicated by arrow; (c) 900V after diode breakdown showing just a small grain. Other parts of the SiC crystal are diffracted to different positions on the X-ray film. The white contrast features are due to the metal leads absorbing the X-ray beam.

Defect delineation study performed using hard X-rays at Argonne's Advanced Photon Source (APS).

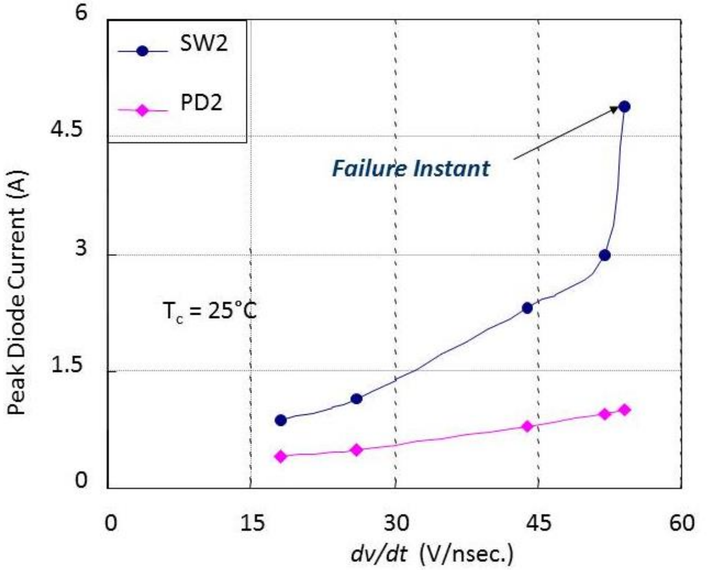
At 900V reverse bias, TSDs in the vicinity of the metal-semiconductor junction were excited and acted as charge generation centers that caused diode breakdown.

K. Shenai *et al*, *Science* (to be published)

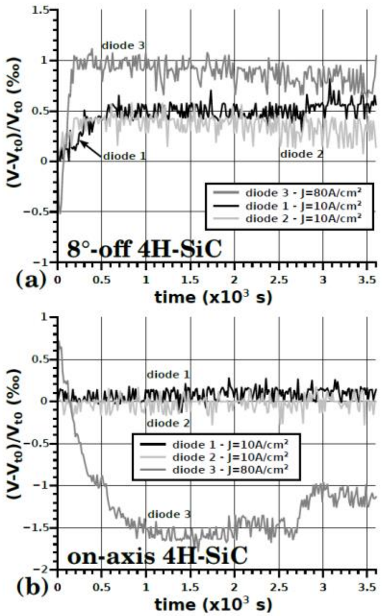
Reliability Evaluation of SiC Power Diode

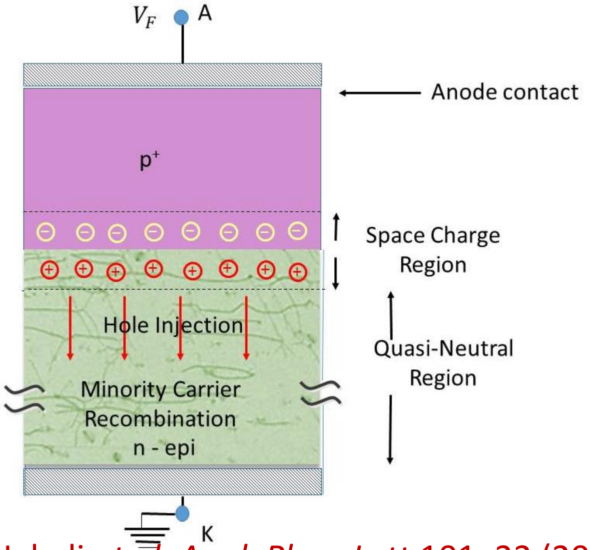


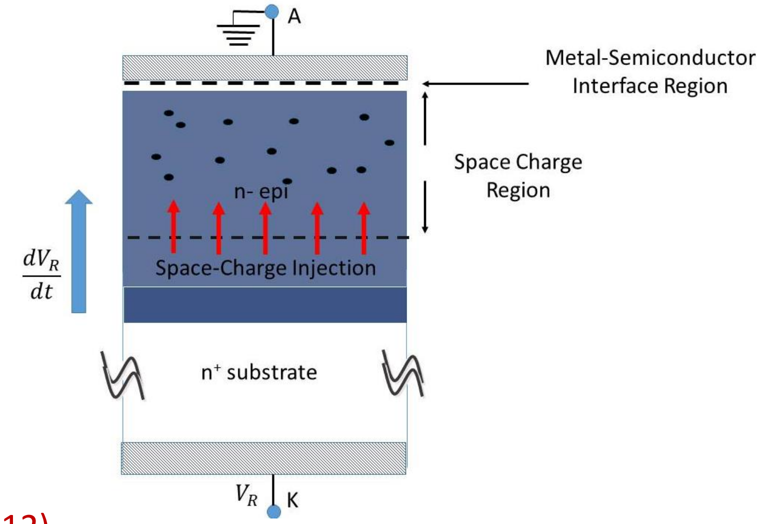
Shenai *et al*, *IEEE Proc.,* 35-52, Jan. 2014



Acharya and Shenai, *PET Conf*., 672-277 (2002)

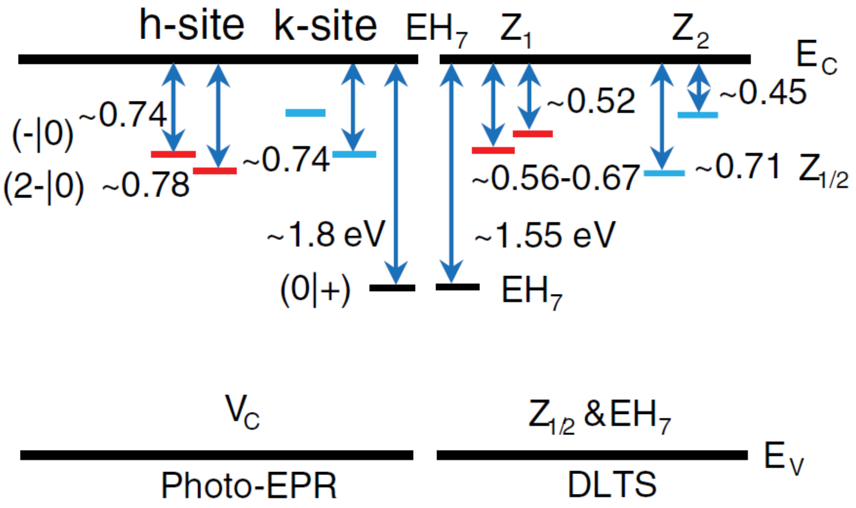


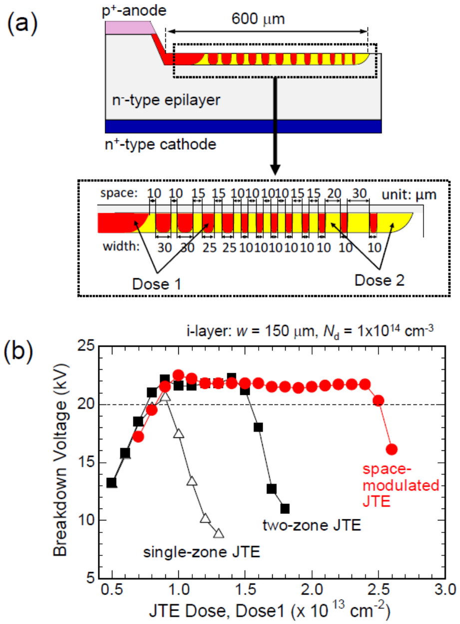


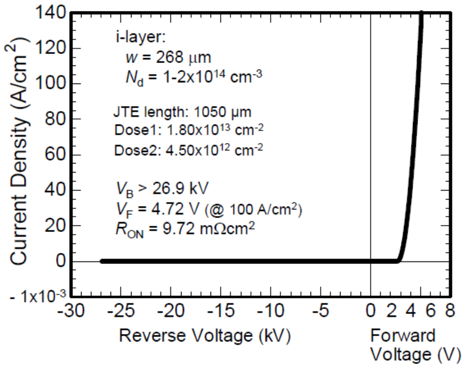


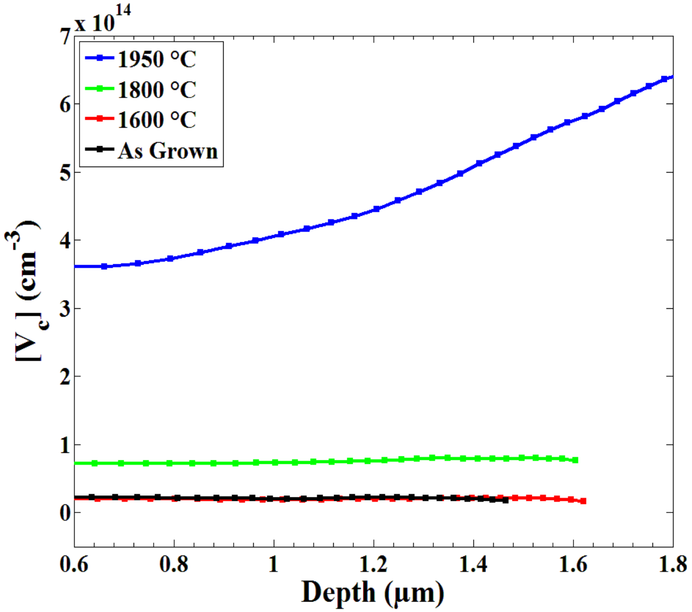
Jabali *et al*, *Appl. Phys. Lett.*101, 22 (2012)

Point Defects in Epitaxial SiC Layers

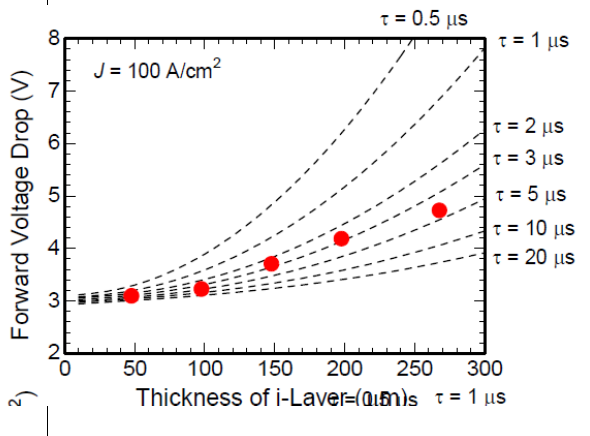


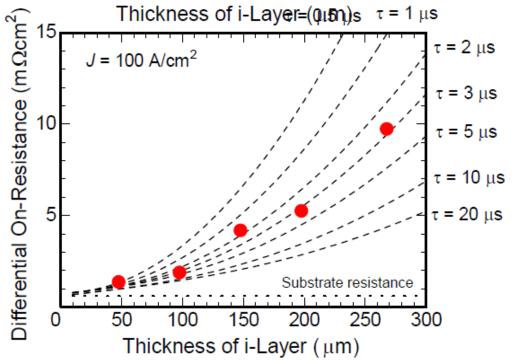






Lovlie *et al*, *J. Appl. Phys.* 111, 103719(2012)

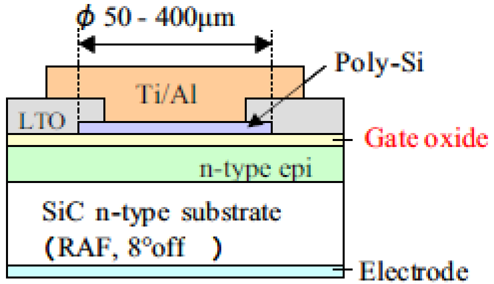


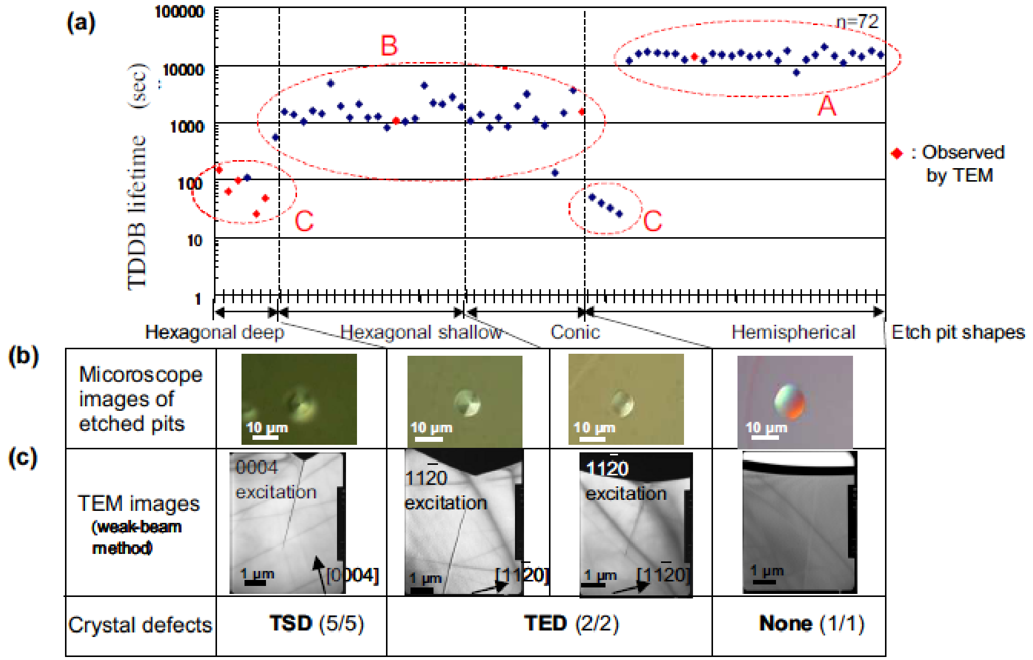


Kaji *et al*, *IEEE TED*, Feb. 2015

Influence of Threading Dislocations on Lifetime of Gate Thermal Oxide in SiC MOSFETs

Yamamoto et al, Mater. Sci. Forum., 717-720, pp 477-480, (2012)

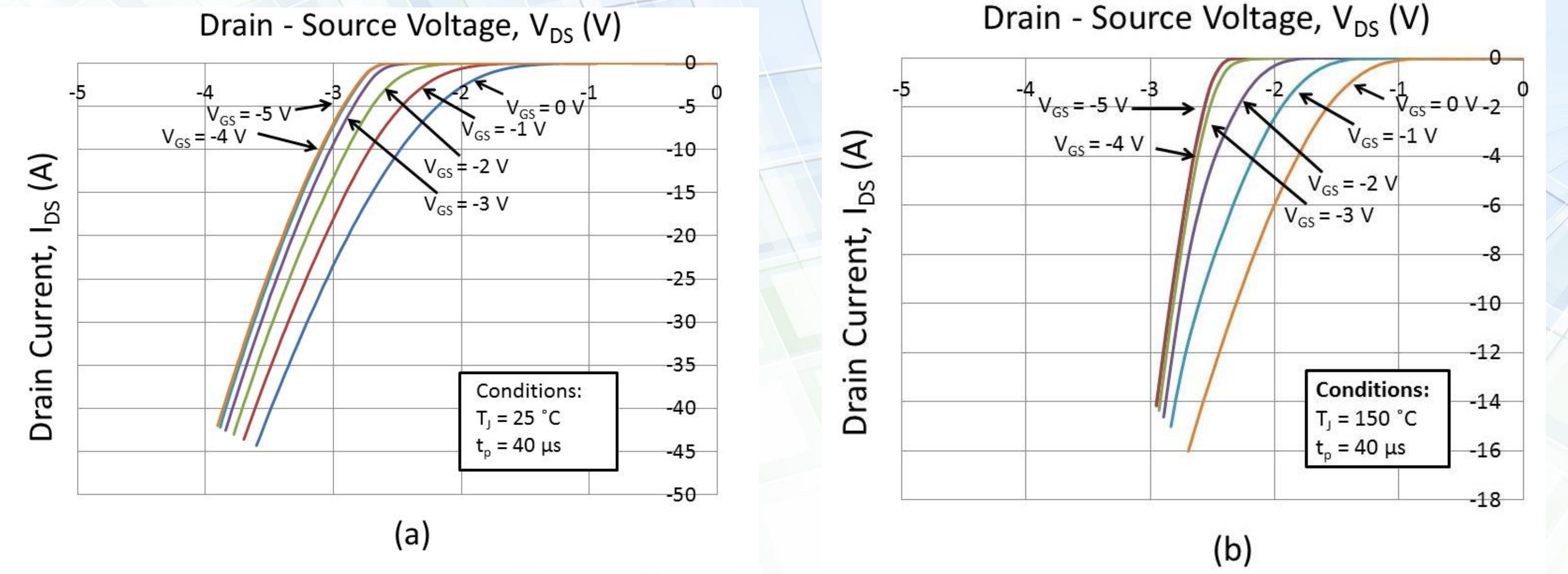




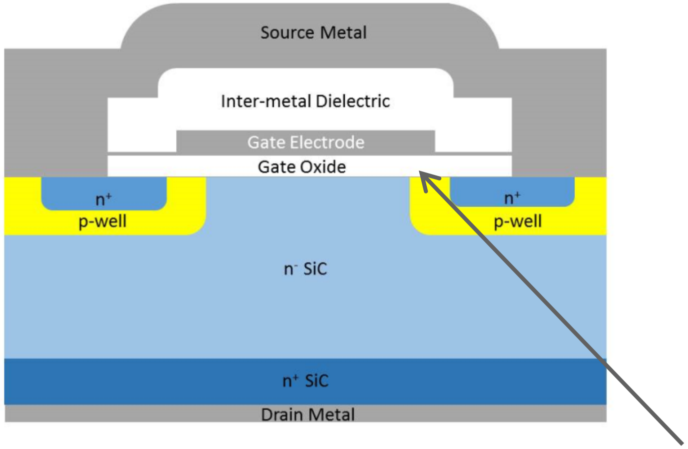
Time Dependent Dielectric Breakdown (TDDB) detected through photo-emission. Defects responsible for the breakdown, i.e., at breakdown location revealed by etching and x-sectional TEM:

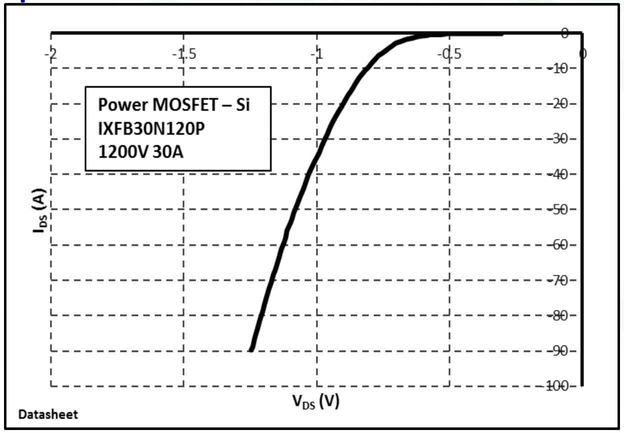
- **Mode A : Intrinsic breakdown (no crystallographic defect);**
- **Mode B: due to TEDs – lifetime shortened by one order of magnitude;**
- **Mode C (shortest Lifetime): due to TSDs – lifetime shortened by two orders of magnitude**

Body Diode On-State Characteristics of SiC MOSFETs



Commercial 1,200V/50A SiC power MOSFETs





Commercial 1,200V/30A Si power MOSFET

Excessive Gate Oxide Charge

Safe Operating Area (SOA)

IXFB30N120P (Si)

V_{DSS} = 1200V

I_{D25} = 30A

$R_{DS(on)} \leq$ 350mΩ

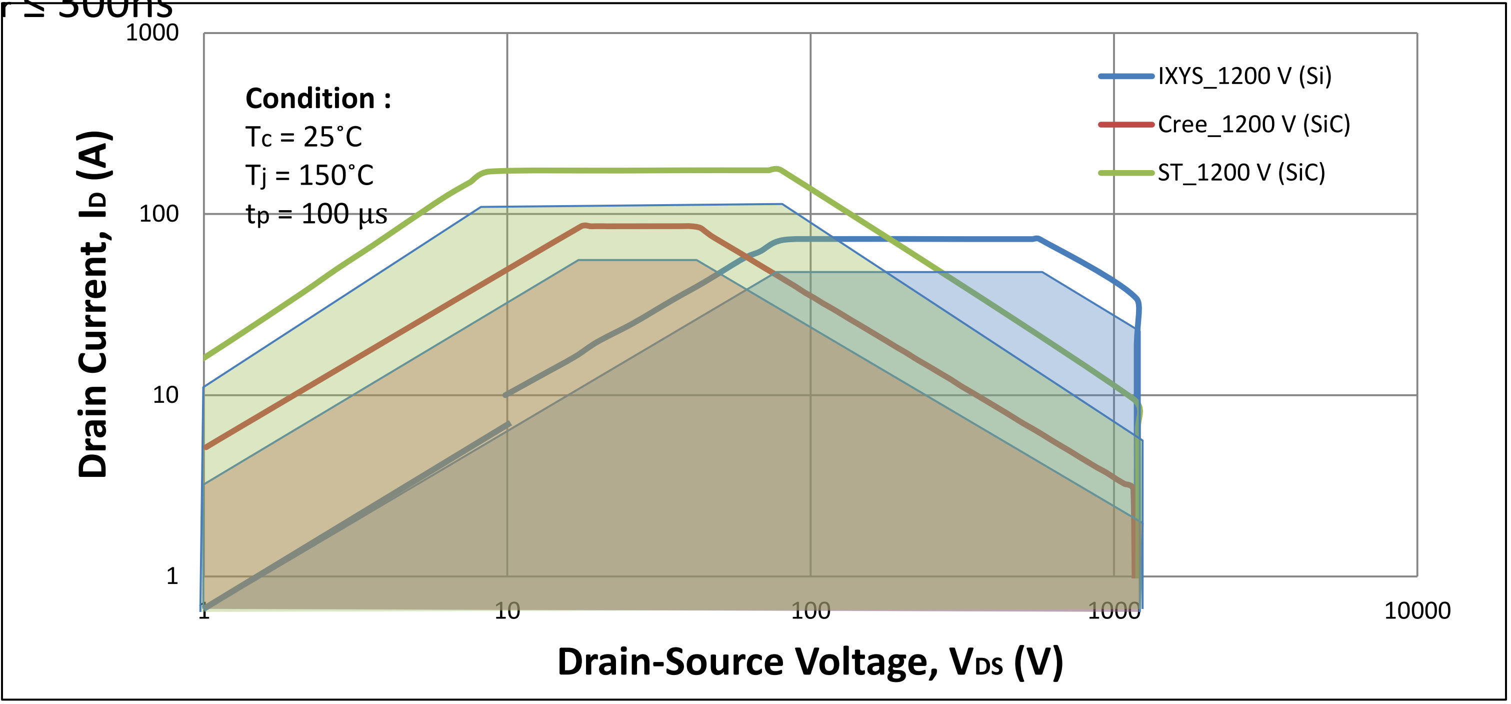
$t_{rr} \leq$ 300ns

C2M0080120D (SiC)

V_{DS}	1200 V
I_D @ 25˚C	31.6 A
$R_{DS(on)}$	80 mΩ

SCT30N120 (SiC)

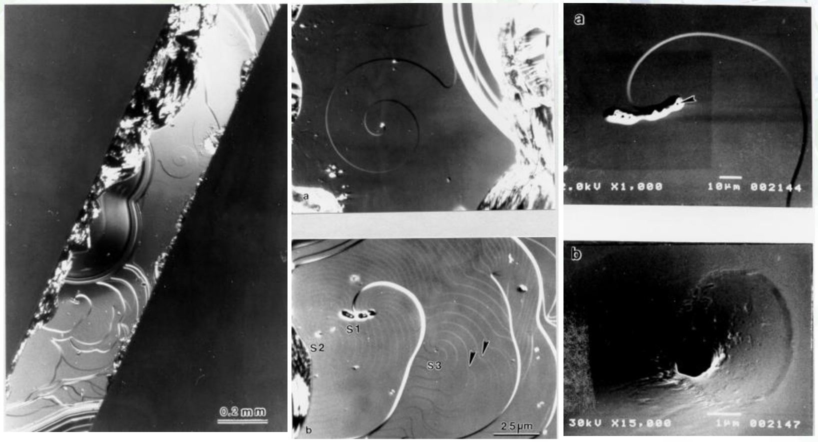
V_{DS}	1200 V
I_D @ 25˚C	45 A
$R_{DS(on)}$	80 mΩ

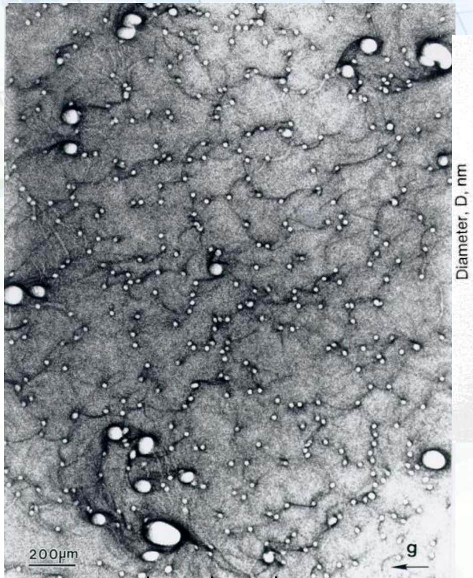

Condition :
T_c = 25˚C
T_j = 150˚C
t_p = 100 µs

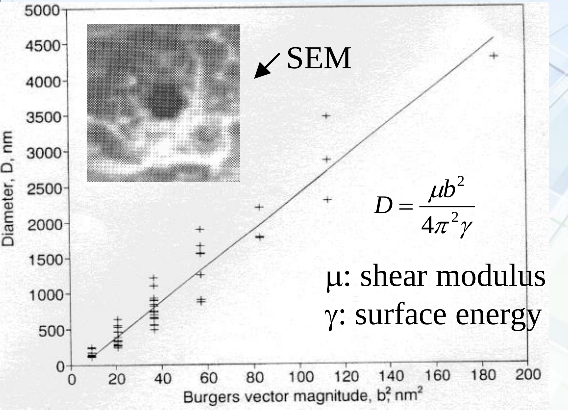
Device type	SOA (in kW)
Silicon (IXYS)	72.4
Silicon Carbide (CREE)	52.7
Silicon Carbide (ST)	59.6

K. Shenai, *IEEE Trans. ED*, Feb. 2015 (to be published)

Dislocations and Micropipes in SiC







$$D = \frac{\mu b^2}{4\pi^2\gamma}$$

μ: shear modulus

γ: surface energy

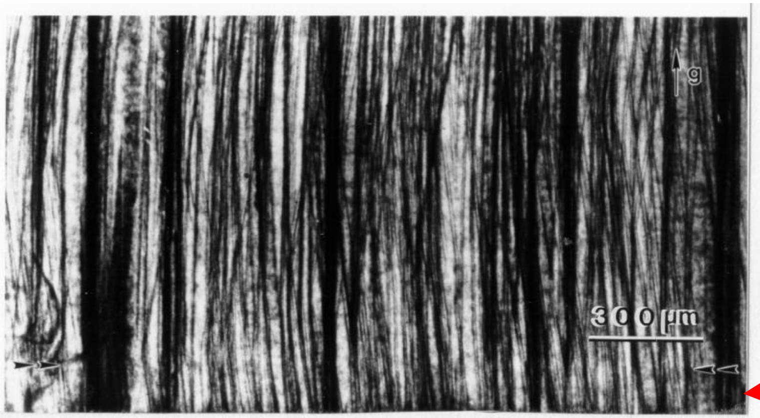
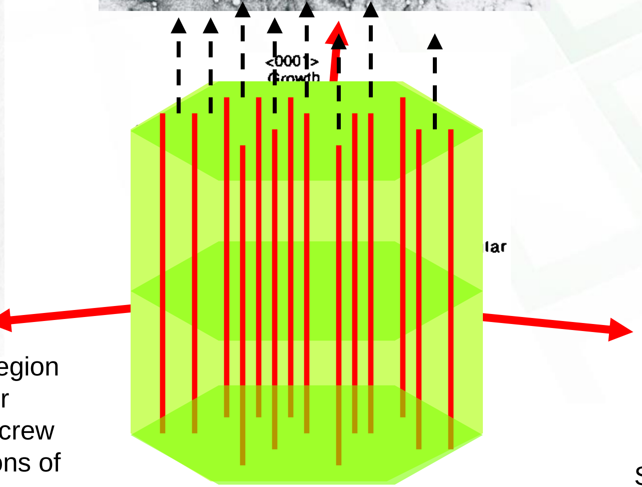
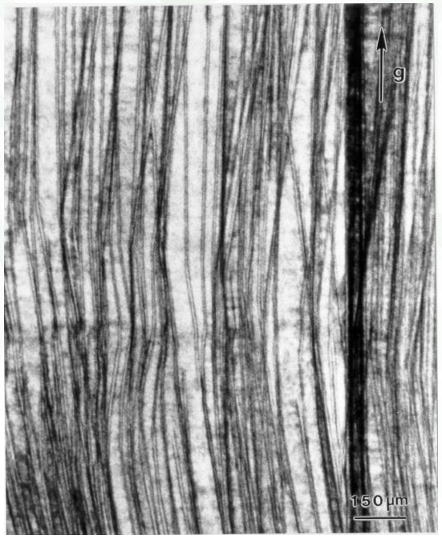


Image from longitudinal slice showing the seed/crystal interface region (indicated by arrows) in a 6H-SiC crystal grown by Physical Vapor Transport. One-to-one correlation can be found between [0001] screw dislocations in the seed and in the newly grown crystal. Dislocations of various Burgers vector can be observed (b=[0006] to b~5[0001])

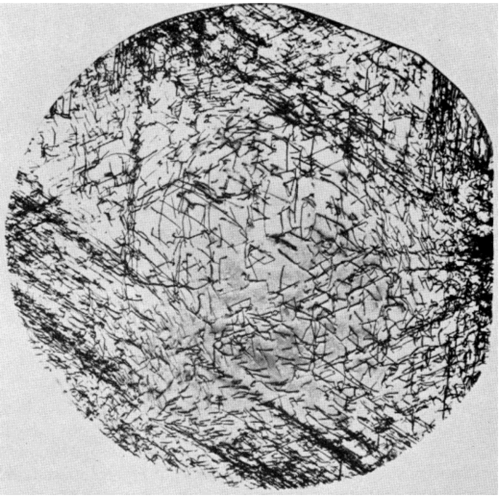




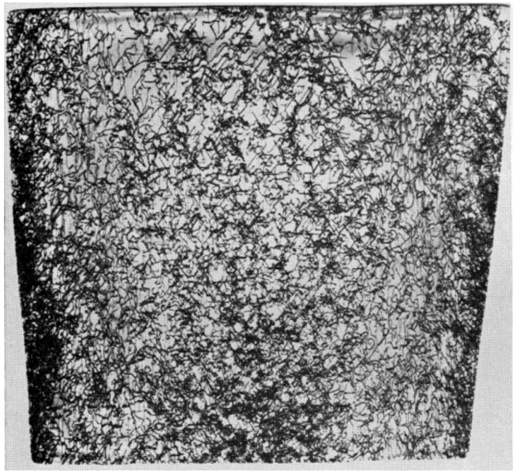
Similar image, lower defect density region.

Dislocations in Silicon

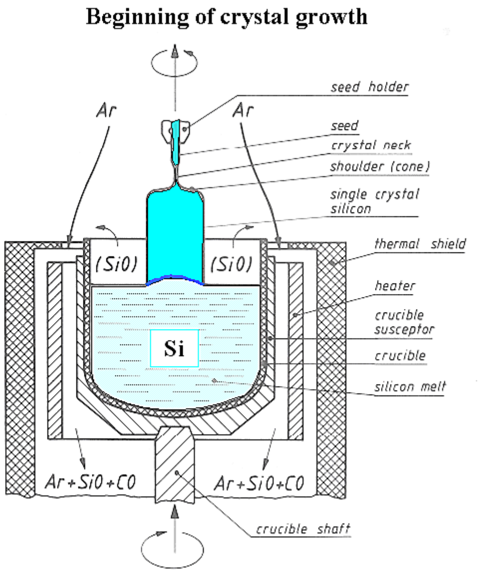
Dislocations in 12 mm diameter Float Zone Si from Jenkinson and Lang, “Direct Observation of Imperfections in Crystals”, Newkirk and Wernick (Eds), Interscience, (1962). (a) 111 slice, -220 reflection; (b) 11-2 axial slice, 111 reflection



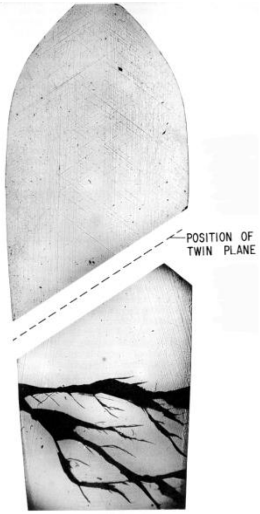
Dislocation Density ~2600 cm^{-2}

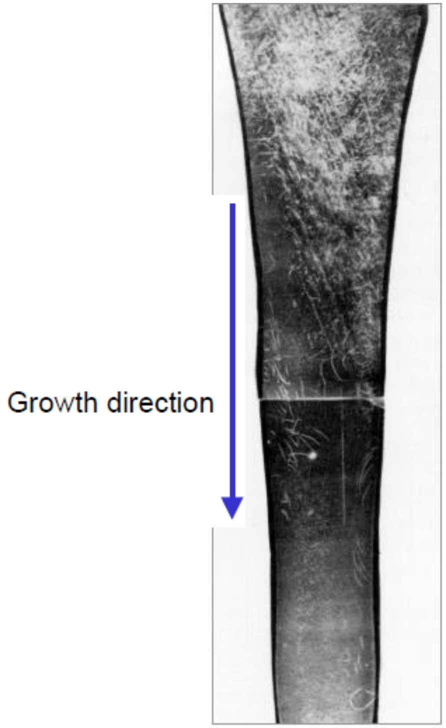


Dislocation Density ~4100 cm^{-2}



IR transmission optical micrograph of Cu decorated dislocations in Czochralski-grown Si (after Dash, in “Growth and Perfection of Crystals”, Wiley, (1958), pp. 361-385).and W.C. Dash, JAP, 459, (1959)





From J. Bohm. Realstruktur von Kristallen. E. Schweizerbart'sche Verlagsbuchhandlung (Nägele u. Obermiller), Stuttgart 1995

Can we build
“Taj Mahal”
on a cracky foundation and
expect it to remain intact for
centuries?

Summary and Recommendations

- Wide bandgap (WBG) power semiconductor devices with superior performance than silicon are instrumental for 21st century energy economy.
- Cost of WBG power devices needs to be reduced, performance optimized, and field-reliability demonstrated.
- Fundamental challenge pertains to the starting material – low defect density, large-area substrates and epi layers are needed – low-temperature growth techniques.
- Radically new homo-epitaxial (for vertical devices) wafer synthesis and MOS channel formation methods need to be developed.
- The role of defects in the ground and excited states needs to be fully understood.
- Failure physics should be investigated and new reliability assessment techniques need to be developed.

Thank you!

Any Questions?