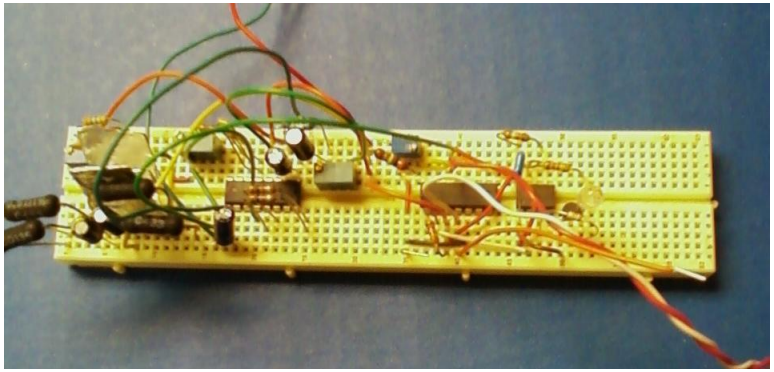
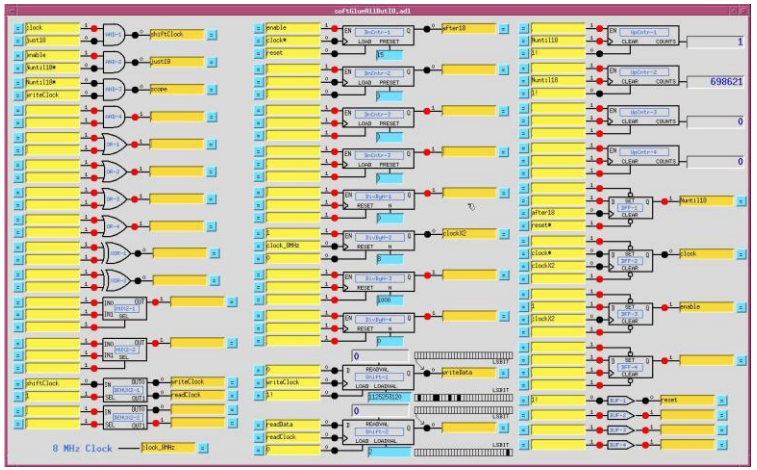
softGlue

(**soft**ware configurable **Glue** electronics)

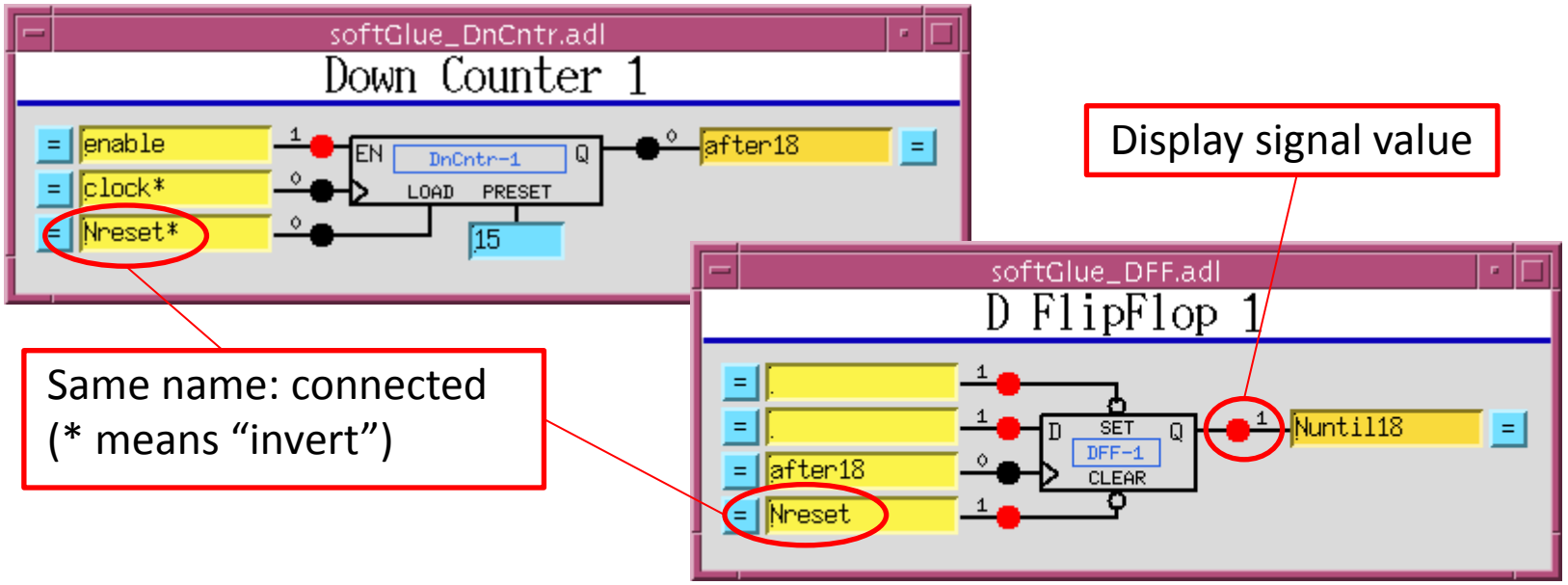
User programmable digital electronics





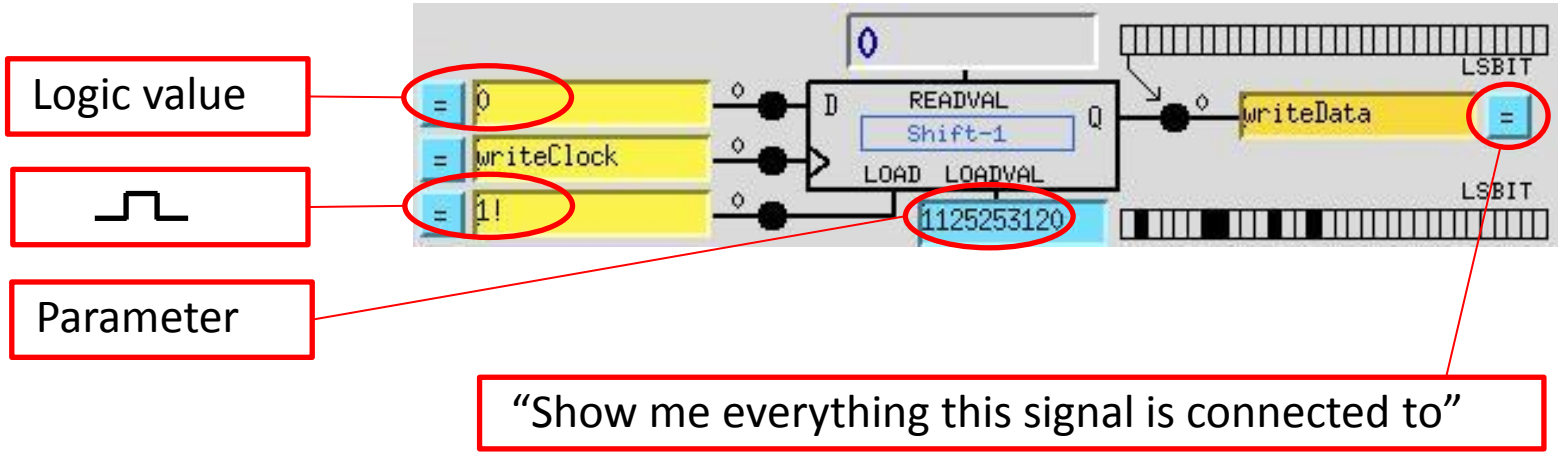
softGlue: at a glance

- Fixed collection of digital logic elements
  - Gates, counters, flip-flops, etc.
  - Loaded into FPGA at boot time
- Programmable connection to field I/O
- Circuit is “wired” by the values of EPICS string PV’s:



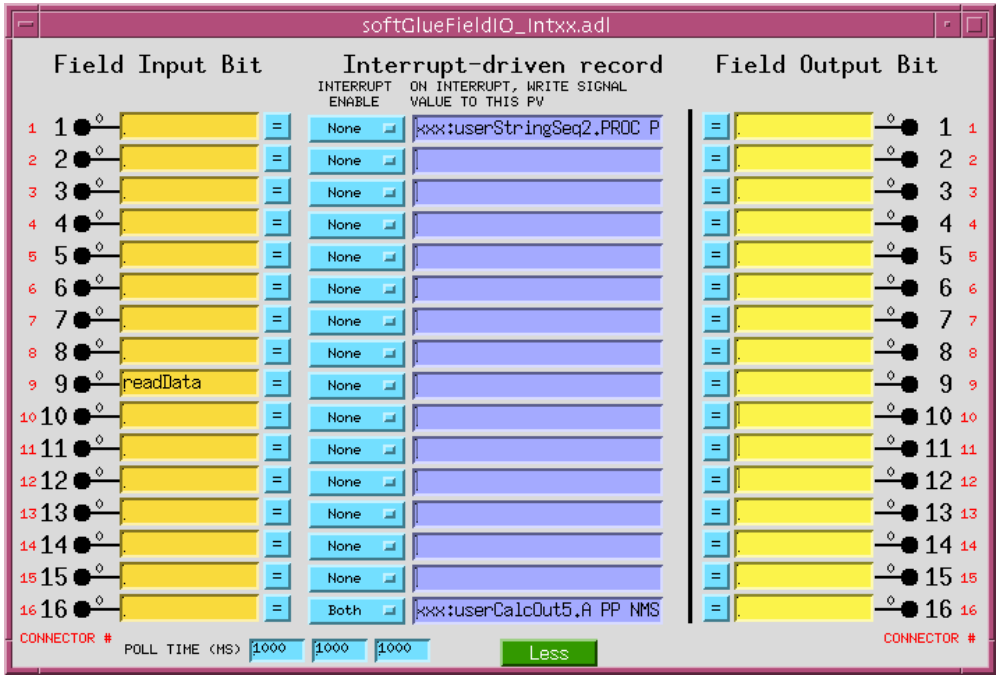
softGlue: EPICS API

- EPICS records, clients can also read and write logic/parameter values directly:



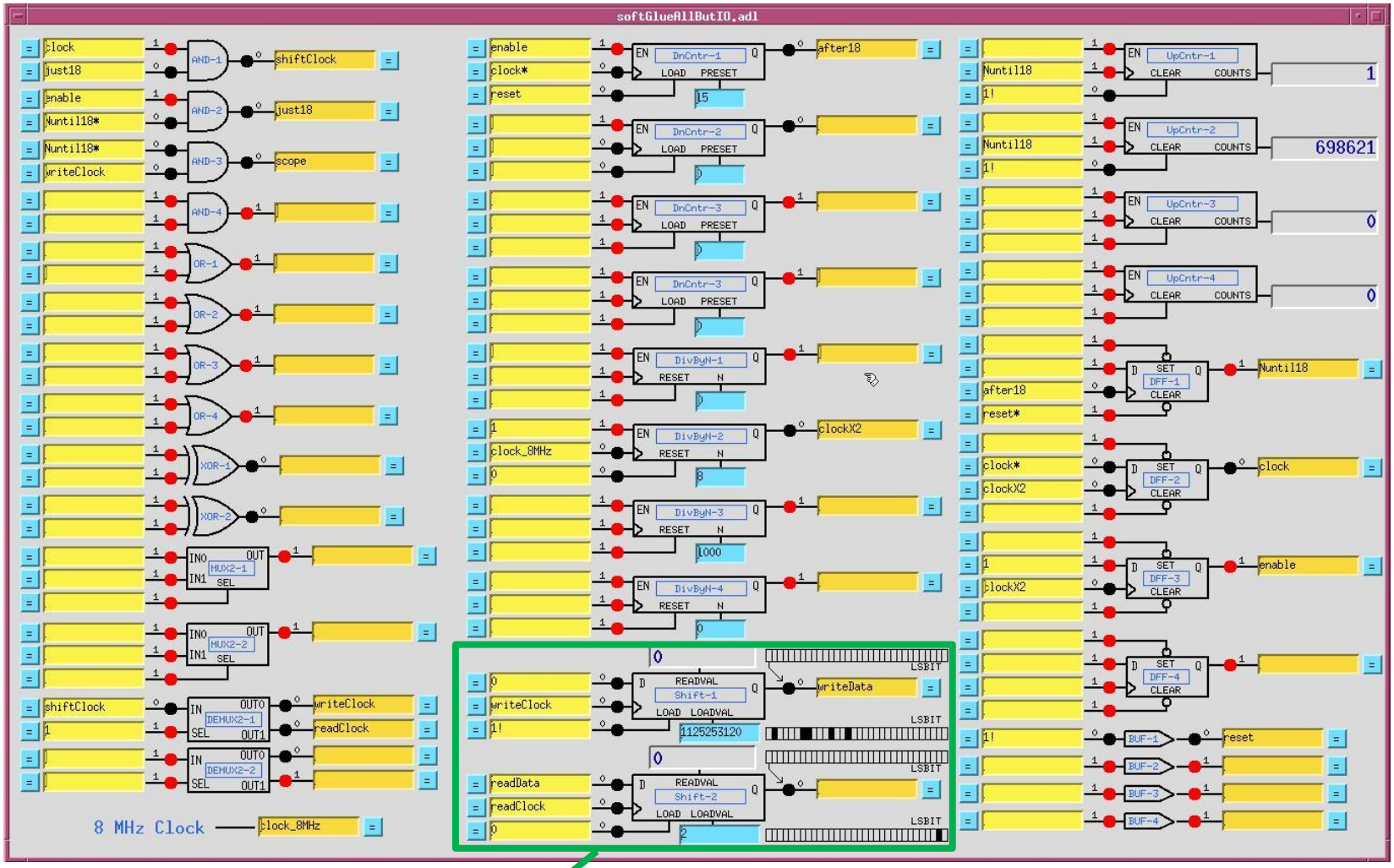
softGlue: field I/O

- Software configurable digital I/O
  - 48-bit TTL (or 24-bit RS-422, LVDS, etc.)
  - field I/O direction specified at boot time
  - Safe, run-time modifiable, interrupt dispatch:
    - On rising edge
    - On falling edge
    - On both
    - On neither



softGlue: FPGA content

Typical collection of electronics elements:



~anything can go here

softGlue: FPGA content

- 4 AND gates
- 4 OR gates
- 4 Buffers
- 2 XOR gates
- 48 field I/O points (inputs or outputs)
- 4 Down counters
- 4 Up counters
- 4 Divide-by-N's
- 4 D Flipflops
- 2 Multiplexers
- 2 Demultiplexers

Also can add custom FPGA content, and provide softGlue interface to selected inputs, outputs, and numeric parameters. Talk to Kurt Goetze.

softGlue: example applications

- Digital I/O
  - With no programming, softGlue functions as 48-bit I/O
- Coordinate digital electronic devices
  - Drive shutters, detectors from motor step pulses
  - Disable data acquisition during motor accel/decel
- Trigger EPICS software on complex I/O events
  - While **A** and **B**, process record on the falling edge of **C**
- Programmable time base for EPICS software
  - Process record at 300 Hz; wait for 470 µs; etc.
- Exceptionally smart oscilloscope trigger
  - Trigger when **A** rises after and within 50 µs of **B,** if motor 7 is moving, the shutter is open, and userStringCalc.AA==“scope”.

softGlue: requirements

- IndustryPack carrier board
- Acromag IP-EP200-series FPGA module
- Field I/O breakout hardware
  - 50-pin ribbon connector
- softGlue EPICS software module
  - softGlue is a synApps module
  - http://www.aps.anl.gov/bcda/synApps/softGlue/softGlue.html
  - softGlue module requires ASYN and IPAC

softGlue: pros and cons

Advantages

- Hardware in close coordination with EPICS software
- Software and hardware in the same repository
- Easy to distribute/install hardware
- Autosave user configured circuitry
- Convenient, standard platform for developer-engineered circuitry
- Easy to implement/deploy experiment-specific circuitry

Limitations

- Only 15 signal names
- Field I/O signals are not maintained during VME reset.
- IP-EP201 field I/O requires special care for high-frequency signals.
  - Unterminated TTL, shared ground line, ribbon cable
  - Other IP-EP200-series modules have terminated differential (RS-422 or LVDS) signals.

softGlue: in context

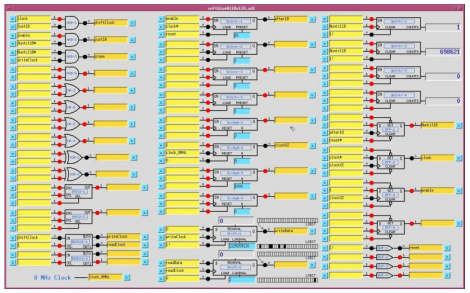
Custom Electronics Options at APS

Low end

B.O.N.E Box

- Always on
- No connection to EPICS
- Limited circuitry
- Difficult to modify
- Difficult to reproduce
- Analog and digital

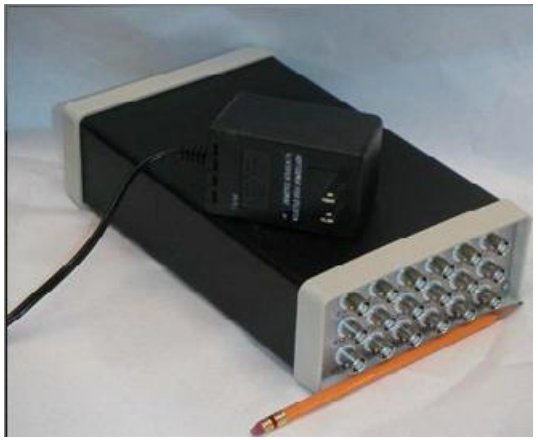
Midrange



softGlue

- Off during reboot
- Connection to EPICS
- Limited circuitry*
- Easy to modify
- Off the shelf*
- Digital only
- For users

High end



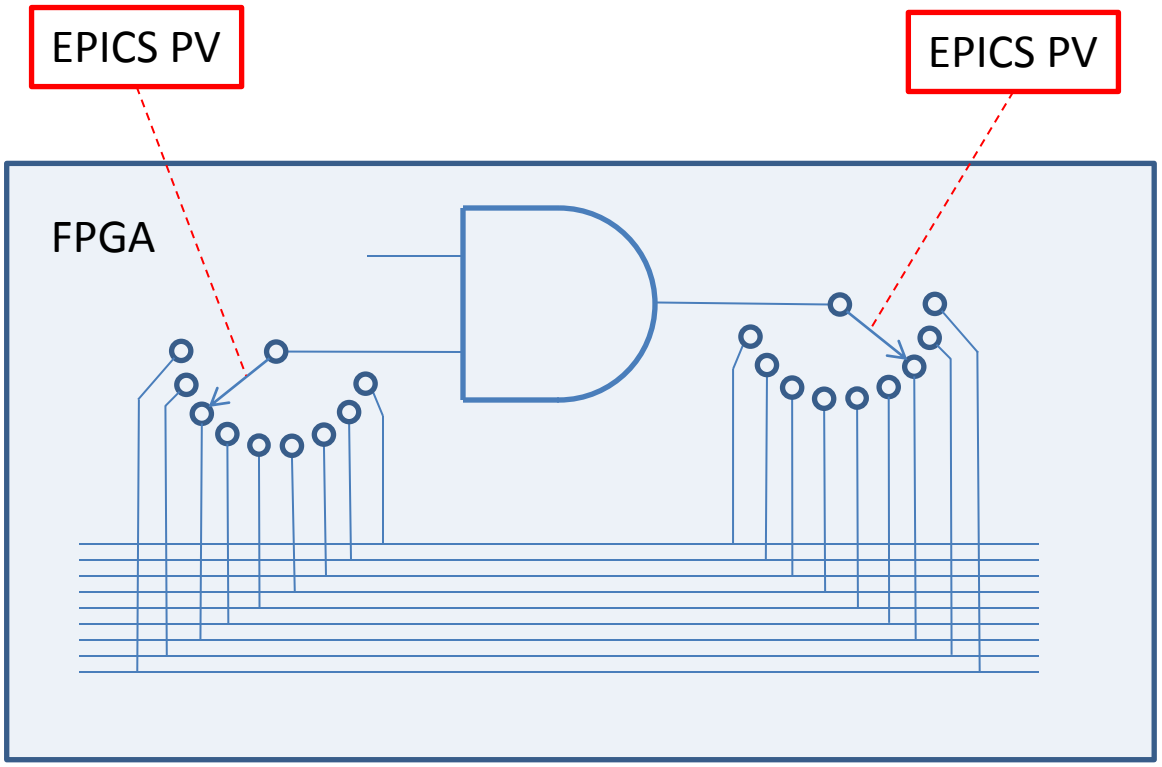
"Generic Digital" Support

- Always on
- No connection to EPICS*
- Unlimited circuitry
- Difficult to modify*
- Difficult to reproduce*
- Analog and digital*
- EE support required

* oversimplification

softGlue: implementation

- The basic idea, schematically:



softGlue: implementation

- Asyn driver
  - Programs FPGA from .hex file
  - Writes to registers implemented in FPGA
  - Manages interrupts
- Asyn device support
  - Standard support for parameter values
  - Custom string support implements signal names
- EPICS database
  - Polls signals for display
  - Marks connected signals for display
- MEDM display files, autosave/BURT request files

softGlue: credits

The cast, in order of appearance:

- Eric Norum – IndustryPack Bridge (interfaces FPGA components to IP/VME bus)
- Marty Smith – EPICS driver, field I/O FPGA
- Kurt Goetze – FPGA content
- Tim Mooney – EPICS application