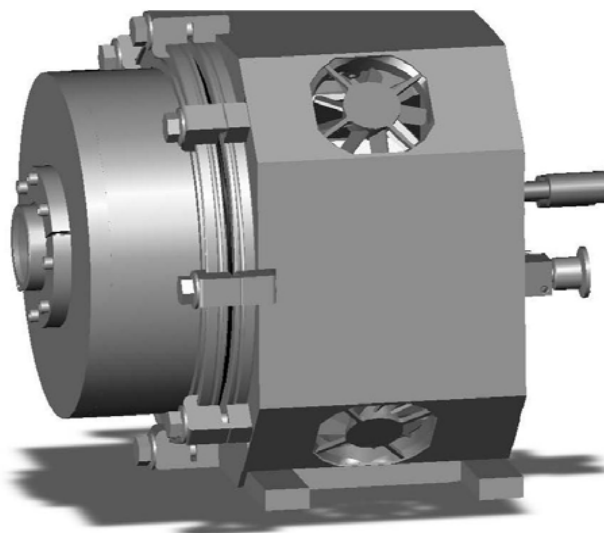




... for a brighter future

APS/LBNL Collaboration on Fast CCD Detectors (Progress Report)



U.S. Department
of Energy

UChicago ►
Argonne_{LLC}



A U.S. Department of Energy laboratory
managed by UChicago Argonne, LLC

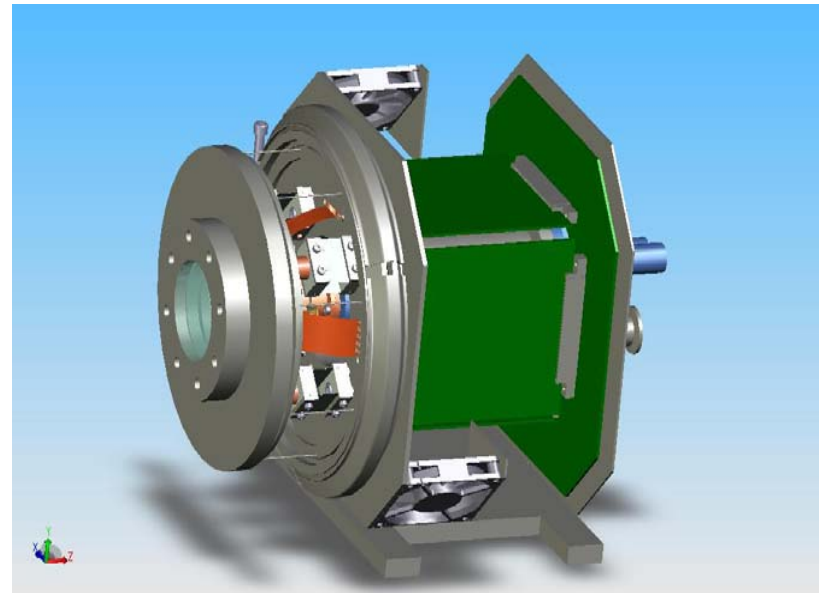
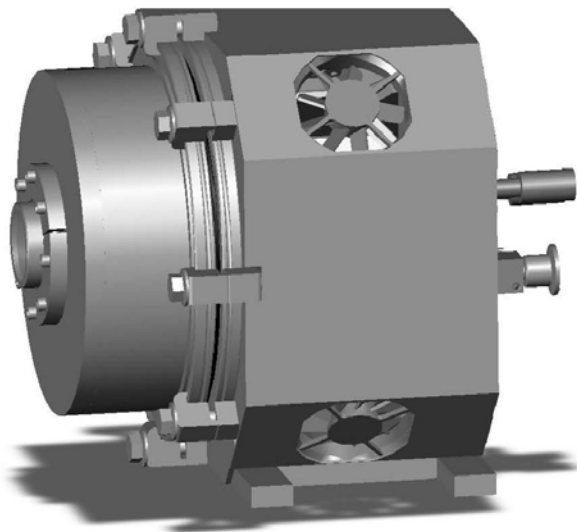
Lead Contacts:

*John Weizeorick from ANL-APS-XSD-Beamline
Technical Support (Detector Pool)*

Peter Denes from LBNL-ALS

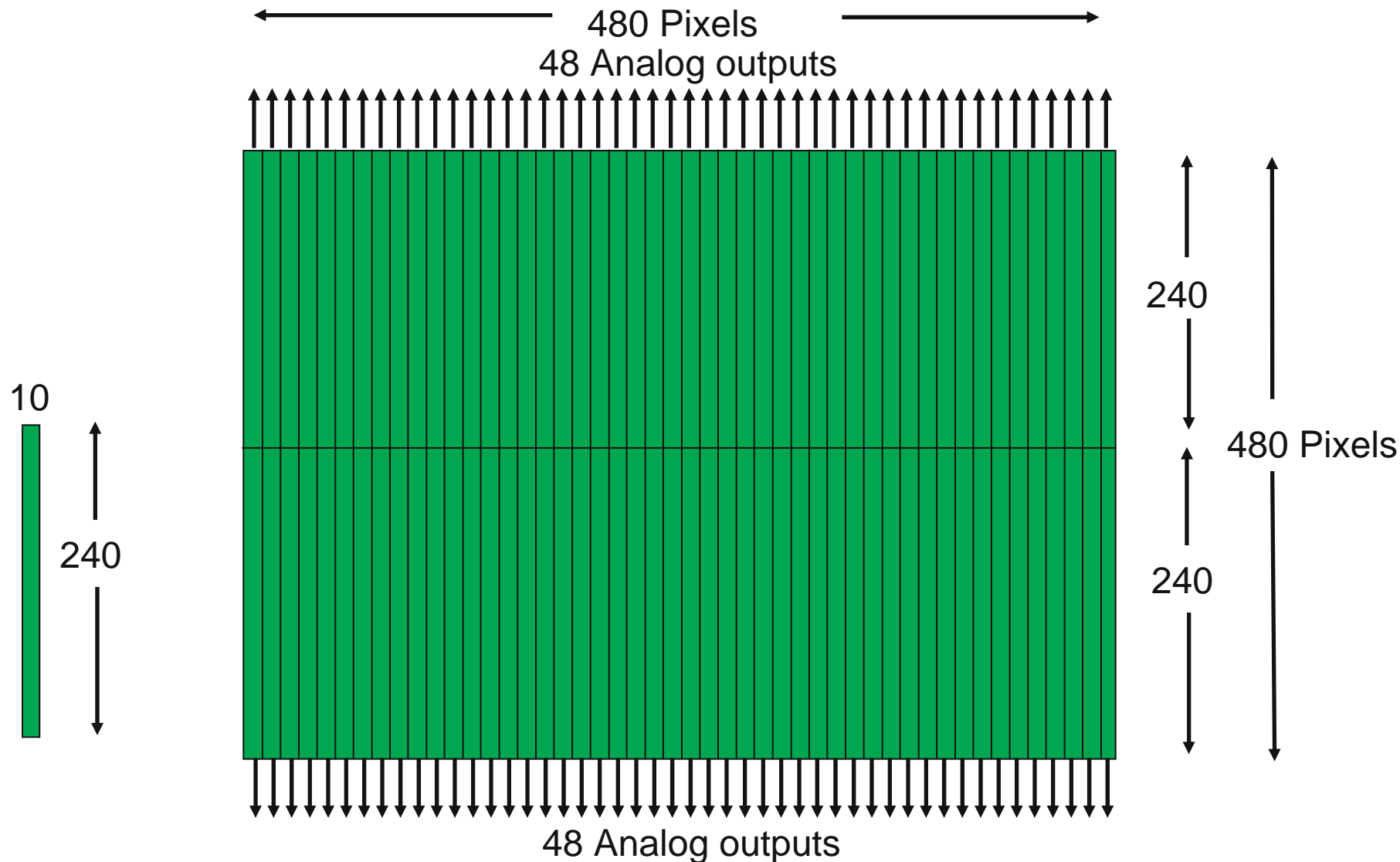
APS/LBNL Collaboration on Fast CCD Detectors (10-25-2006)

- Produce two CCD x-ray detectors using CCD and Readout ICs developed at LBNL
 - Quasi-column parallel CCD with fast readout (96 analog outputs)
 - 480 x 480 (30um pixels), Back-illuminated (Better QE)
 - 200-300 um Thick (Direct detection of x-rays)
 - Readout time of 3.3msec/frame (300 frames per sec)
 - Estimated resolution of 14 bit and full well of 150k electrons
- At APS there is a strong interest from the XPCS (X-ray Photon Correlation Spectroscopy) community



APS/LBNL Collaboration on Fast CCD Detectors

CCD Geometry



APS/LBNL Collaboration on Fast CCD Detectors (10-25-2006)

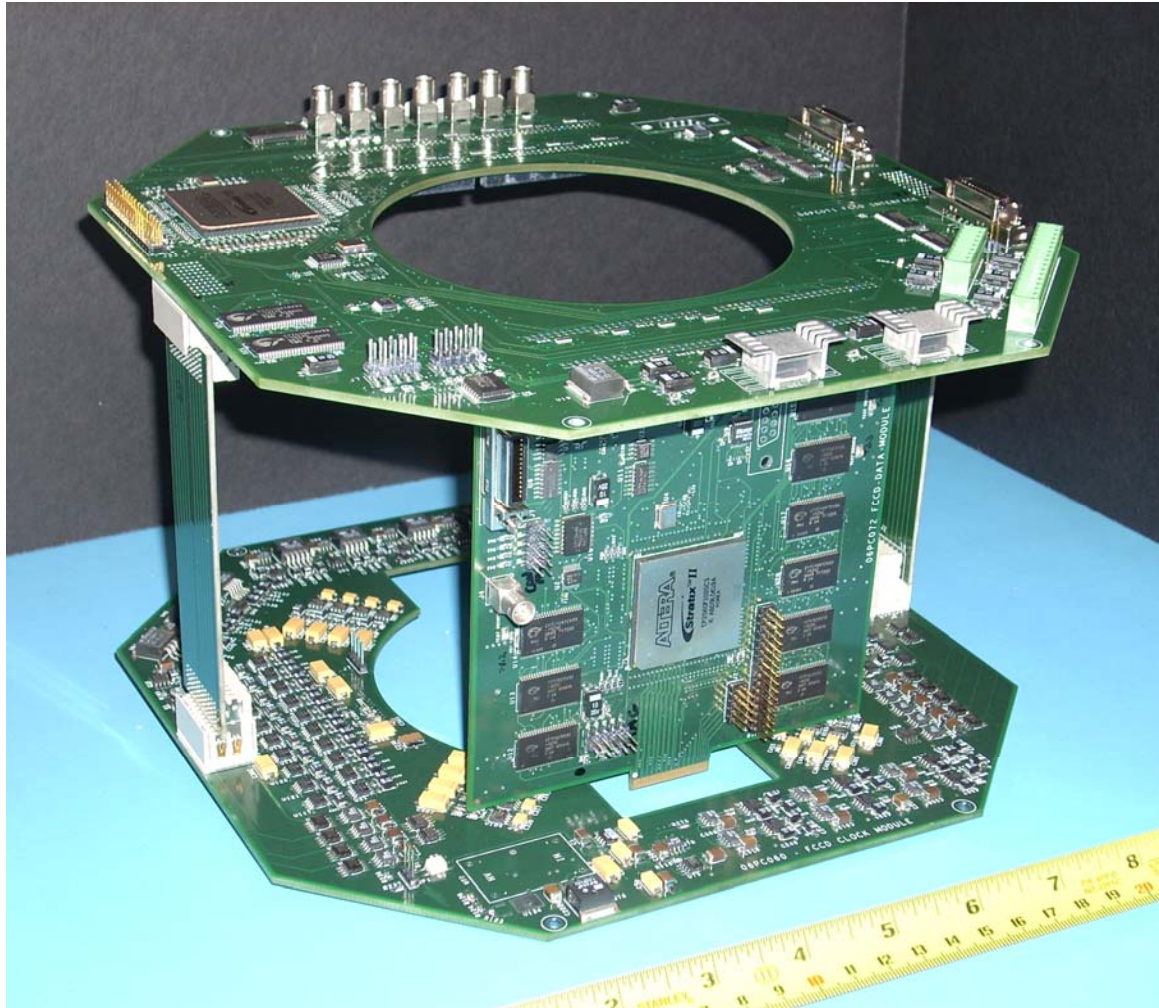
Collaboration

- Divide Task up according to expertise
- Strong Communications - Video Conferences, Email, Phone
- Travel to integrate hardware
 - February 2008 – Test APS clock and interface modules @ LBNL
 - June 2008 – System Integration of Prototype @ LBNL

- LBNL
 - Quasi-column parallel CCD
 - fCRIC readout chip
 - CCD Assembly
 - Mechanical Housing
 - *Vacuum Chamber*
 - *Cooling*
- APS
 - Back End Electronics
 - *Interface Module*
 - *Data Module*
 - *Clock Module*
 - *Power Supply*
 - User Interface, Computer, Commercial Frame Grabber

APS/LBNL Collaboration on Fast CCD Detectors (9-13-2007)

■ Back End Electronics



APS/LBNL Collaboration on Fast CCD Detectors

- GUI to control backend electronics during development phase

The screenshot displays the 'FCCD Interface Module' GUI. It features several control panels:

- Detector OFF-Line:** Includes 'Single Exposure' and 'Exposure Mode' (Single/Repeat) buttons. Exposure Time is set to 100 msec and Repeat Cycle time to 1000 msec. 'CCD ON' and 'CCD OFF' buttons are present, with 'CCD OFF' currently selected and 'OFF' displayed.
- Voltages:** A grid of input fields for various voltages: +Clk Voltage (0V->+10V), -Clk Voltage (-10V->0V), HV (0->99V), OTG (0->5V), V(1->3), TgClk, H(1->3), SwtClk, RgClk, VDDRST (0->-15V), VDDOUT (0->-25V), NGD (-10V->+10V), NCON (-10V->+10V), and GAURD (-10V->+10V).
- Serial Port Status:** Port is COM2, Baud is 115200. Open/Close buttons are available.
- Clock Waveforms:** A list of digital signals with their current values (all 0000000000000000): Hclk1-idle, Hclk2-idle, Hclk3-idle, Sw-idle, Rg-idle, Vclk1-idleRd, Vclk2-idleRd, Vclk3-idleRd, Tg-idleRd, Hclk1-Rd, Hclk2-Rd, Hclk3-Rd, Sw-Rd, Rg-Rd, and ConvT-Rd.
- State Parameters:** A table showing parameters S0 through S7 in hexadecimal. All values are 00.

State Parameters	S0	S1	S2	S3	S4	S5	S6	S7
NUMBERS IN HEX!								
25nsec_per_tick	00	00	00	00	00	00	00	00
ticks_per_state	00	00	00	00	00	00	00	00
passes_per_state	00	00	00	00	00	00	00	00
next_state	00	00	00	00	00	00	00	00
loops_per_state	00	00	00	00	00	00	00	00
loop_state	00	00	00	00	00	00	00	00

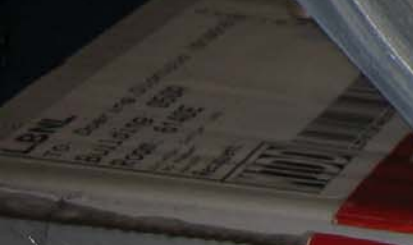
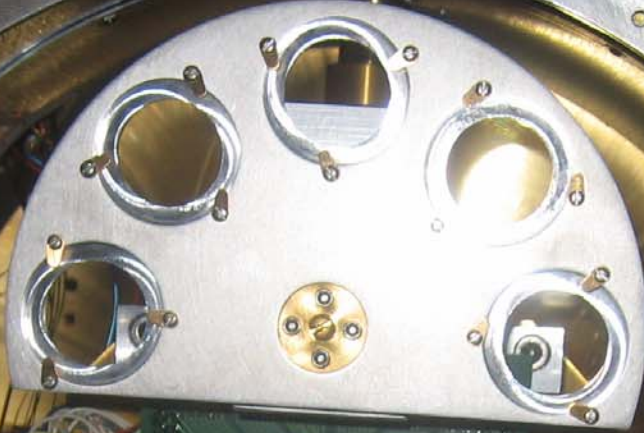
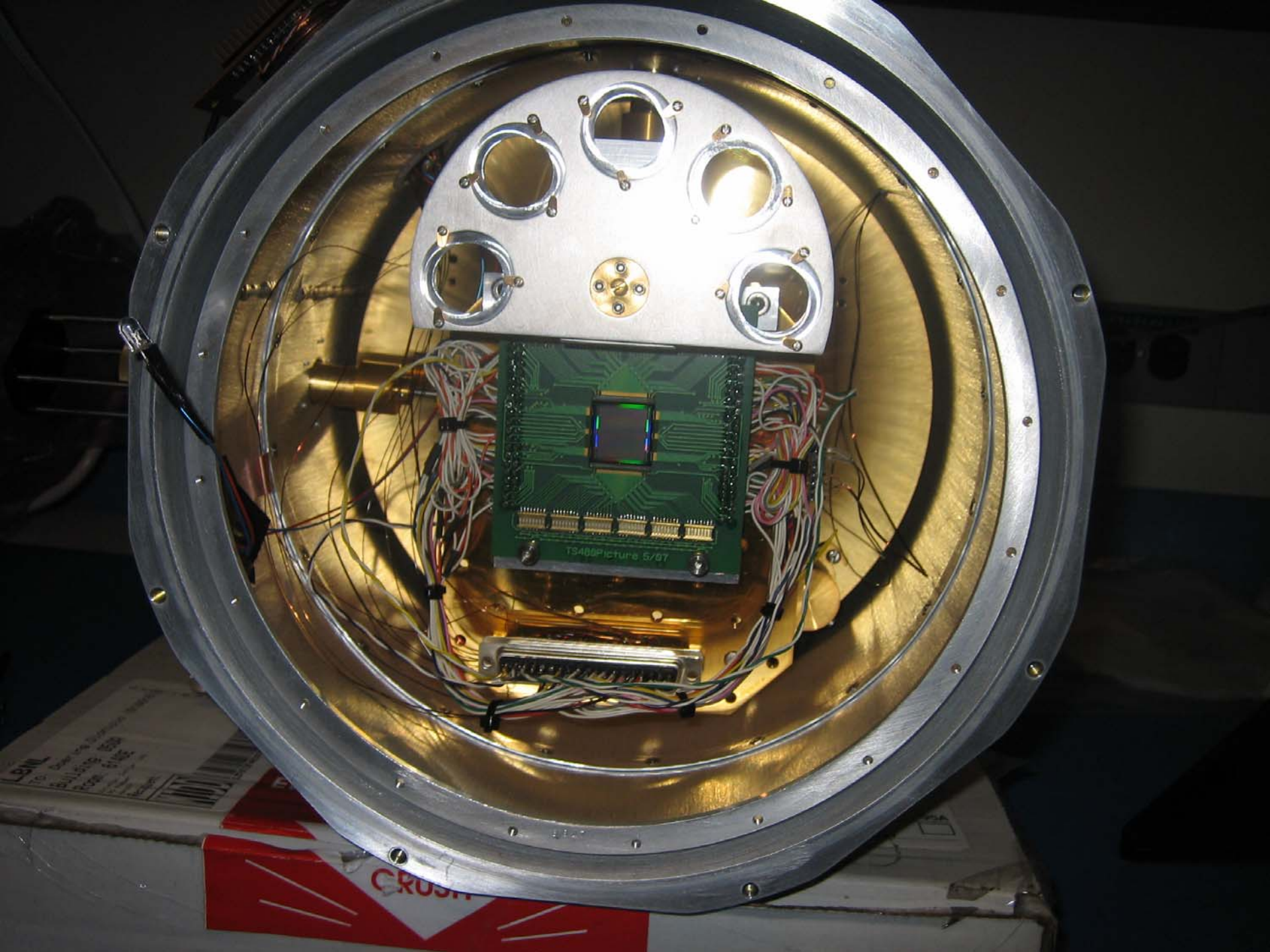
Legend for State Parameters:

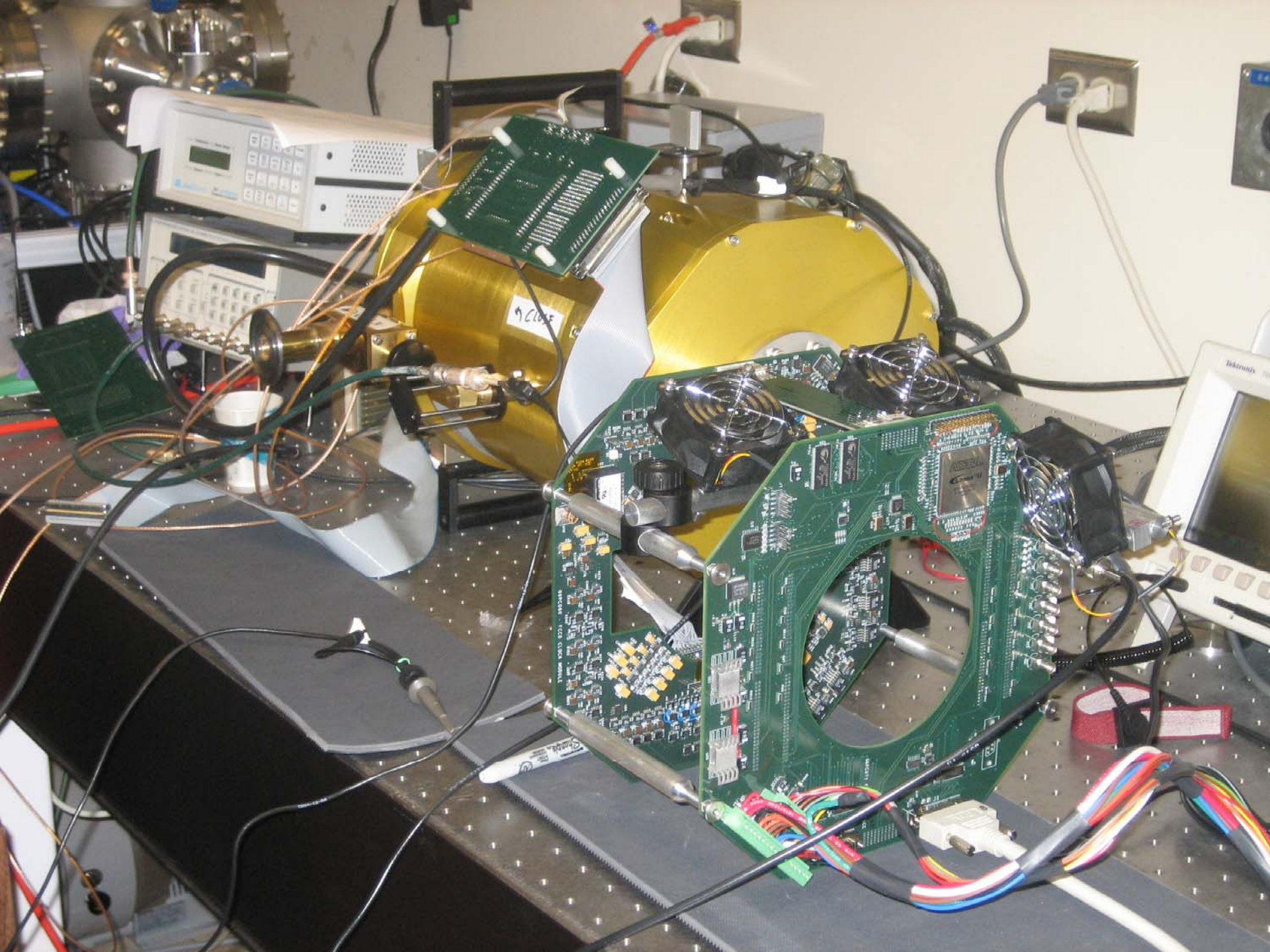
- S0 - Vertical Shift during idle
- S1 - Horizontal Shift during idle
- S2 - Exposure - after S0 or S1 finishes
- S3 - Horizontal Read
- S4 - Vertical Shift during read

At the bottom, there is a 'Command Out' field with the hex command '41' and a 'MESSAGE BOX' indicating 'Port Closed'.

APS/LBNL Collaboration on Fast CCD Detectors (2-20-2006)

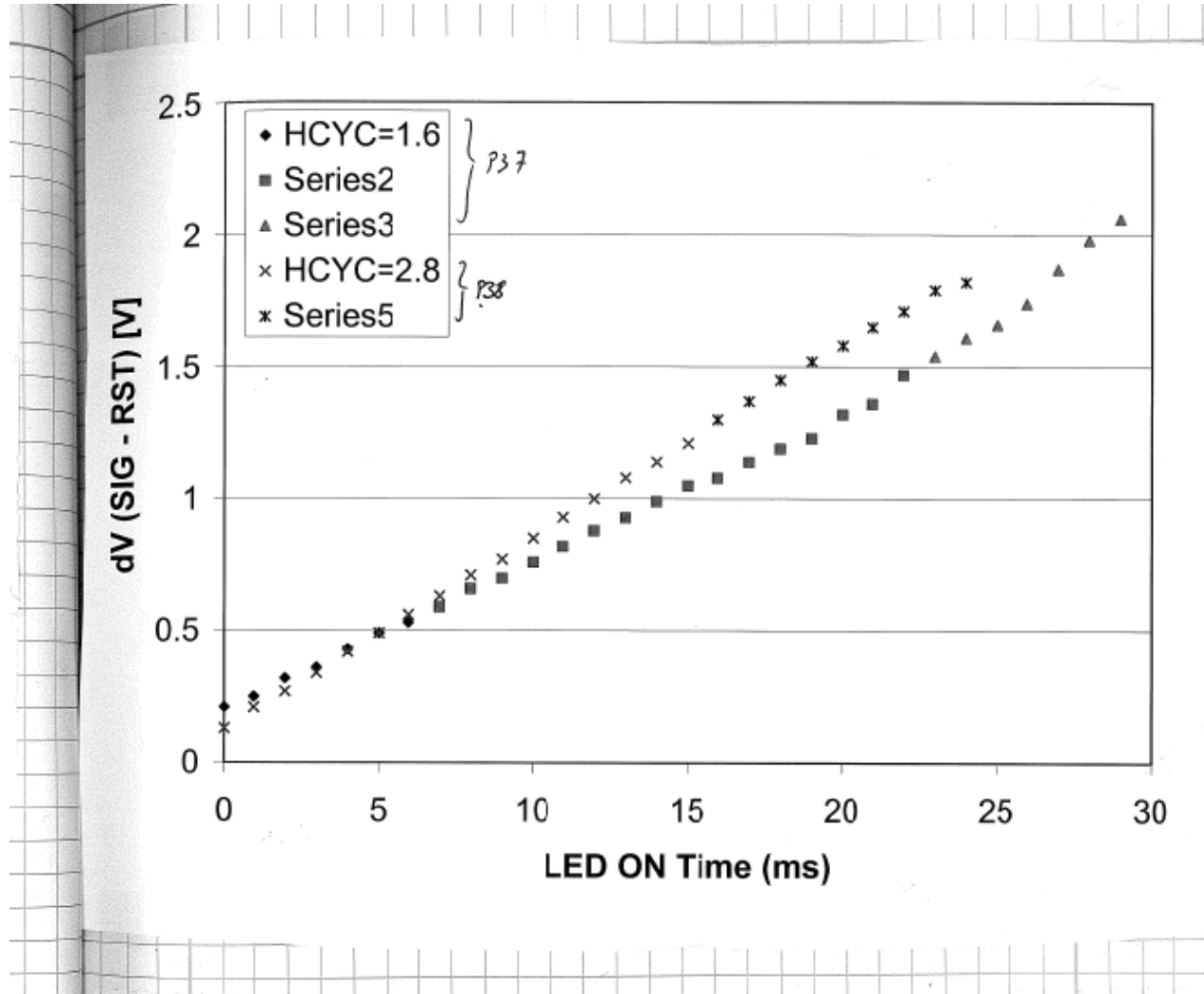
- February 2008 Trip to LBNL
 - Goal
 - *Test CCD with APS's clock module*
 - Steps
 - *Put CCD into commercial CCD Dewar*
 - *Hook up APS's clock module*
 - *Debug Problems*
 - *Verify CCD outputs look good by make quick linearity measurements with oscilloscope*





APS/LBNL Collaboration on Fast CCD Detectors

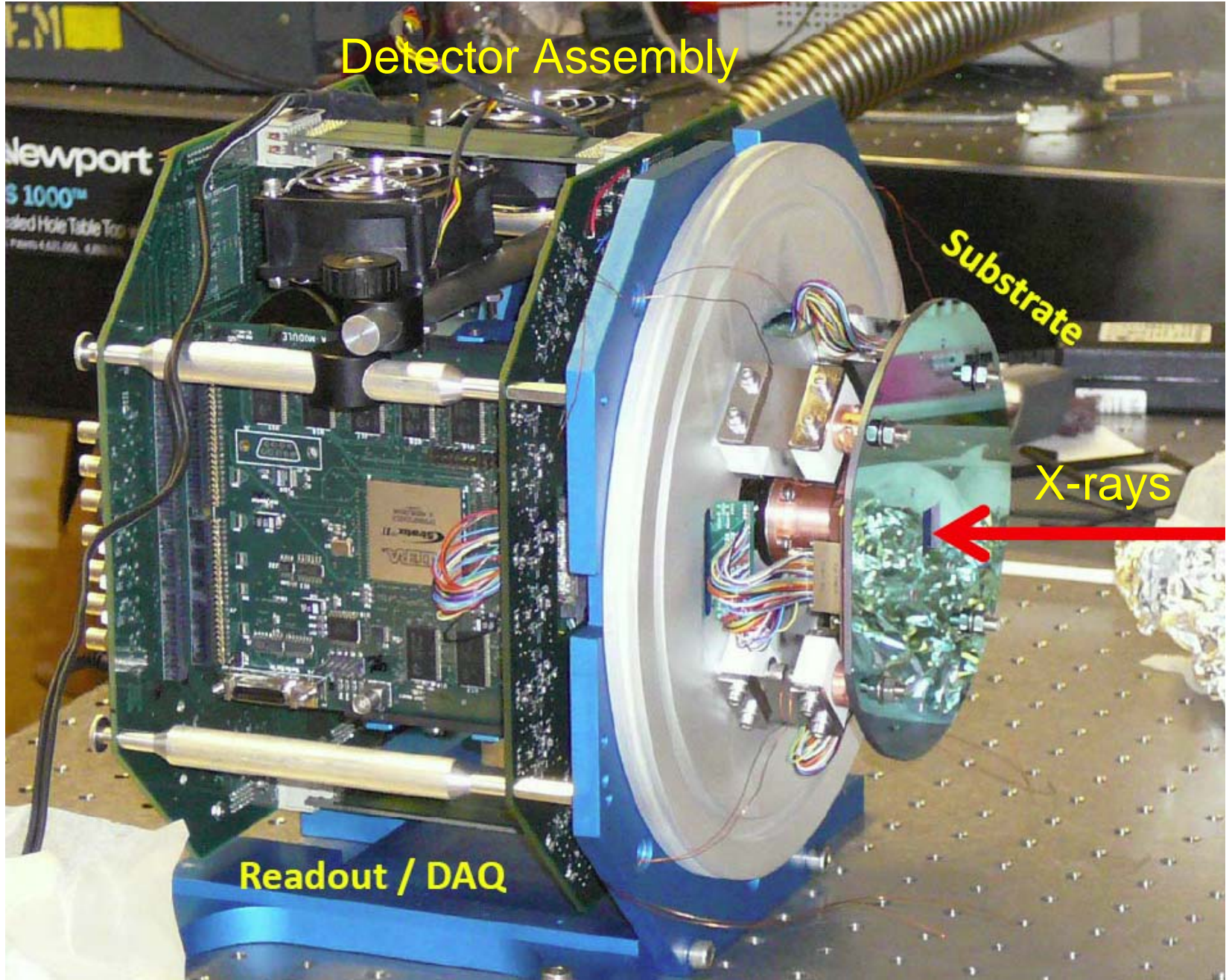
- Linearity check of single pixel with data collected from an oscilloscope



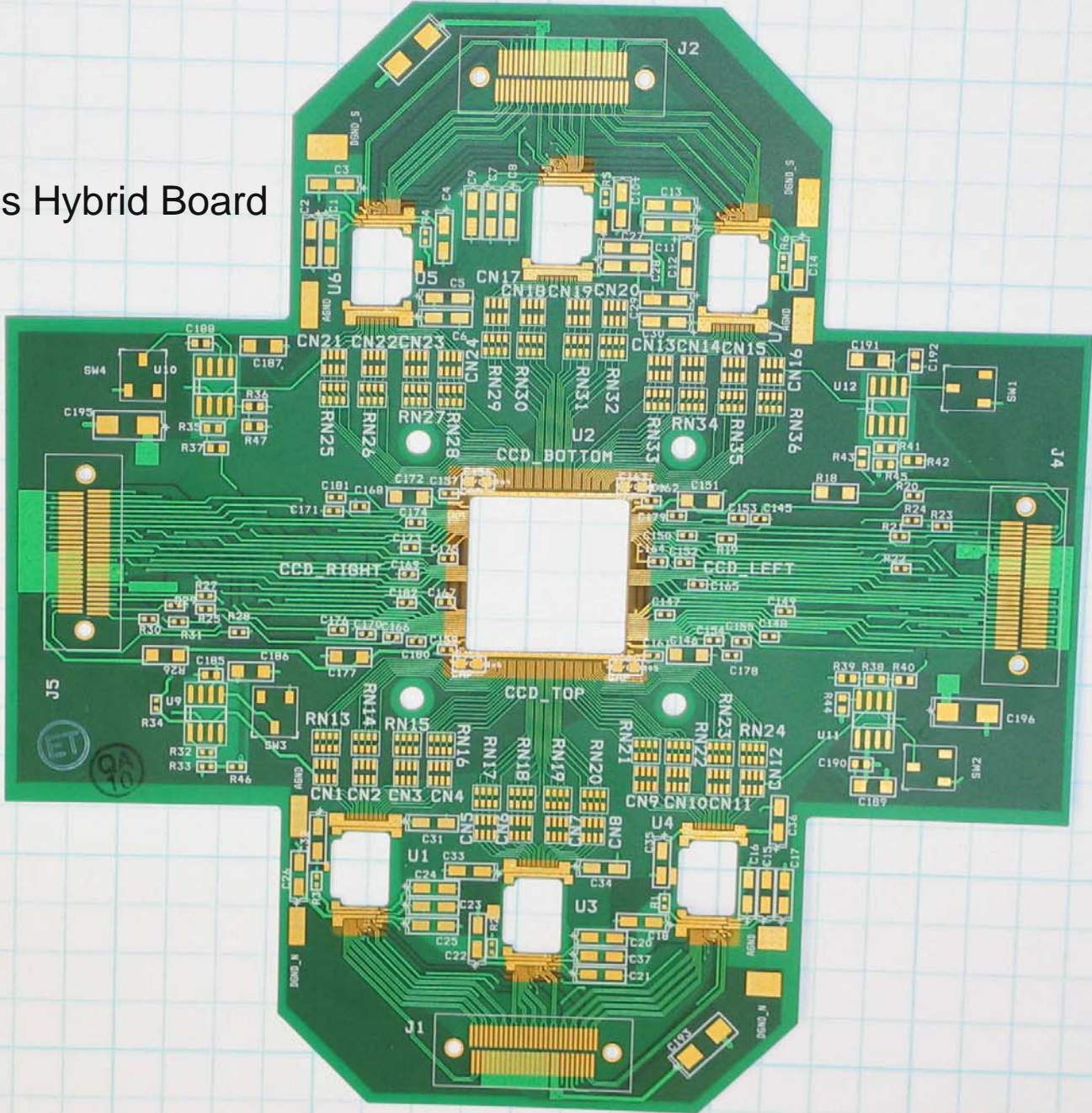
APS/LBNL Collaboration on Fast CCD Detectors

- June 2008 – Trip to LBNL
 - Goal
 - *Integrate whole system and start taking images*
 - Steps
 - *Bring one complete set of all hardware to LBNL*
 - *Assemble all of the parts*
 - *Power it up (Smoke Test)*
 - *Debug Problems*
 - *Start taking images*

Detector Assembly



LBL's Hybrid Board



FCCD Substrate

fCRICs

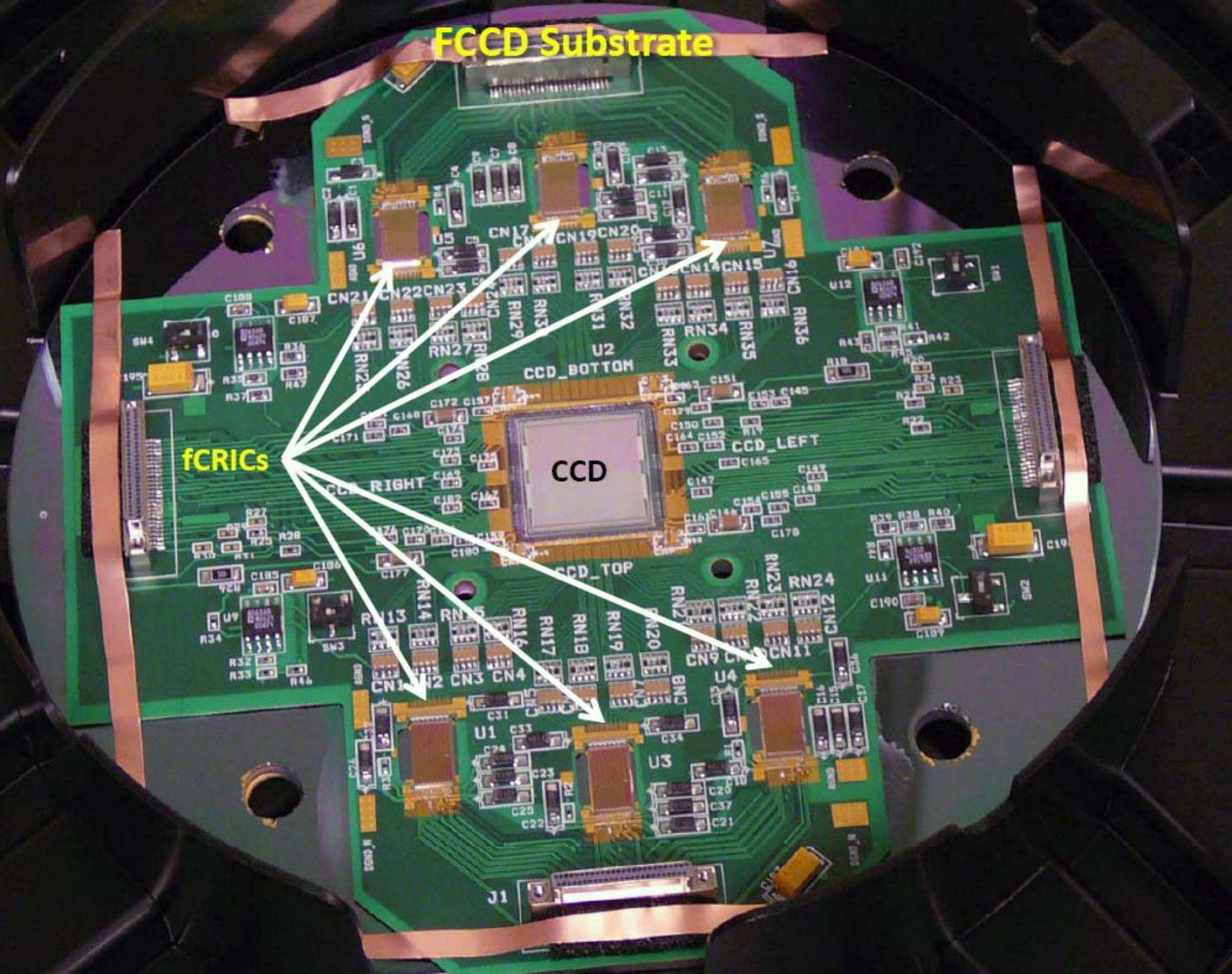
CCD

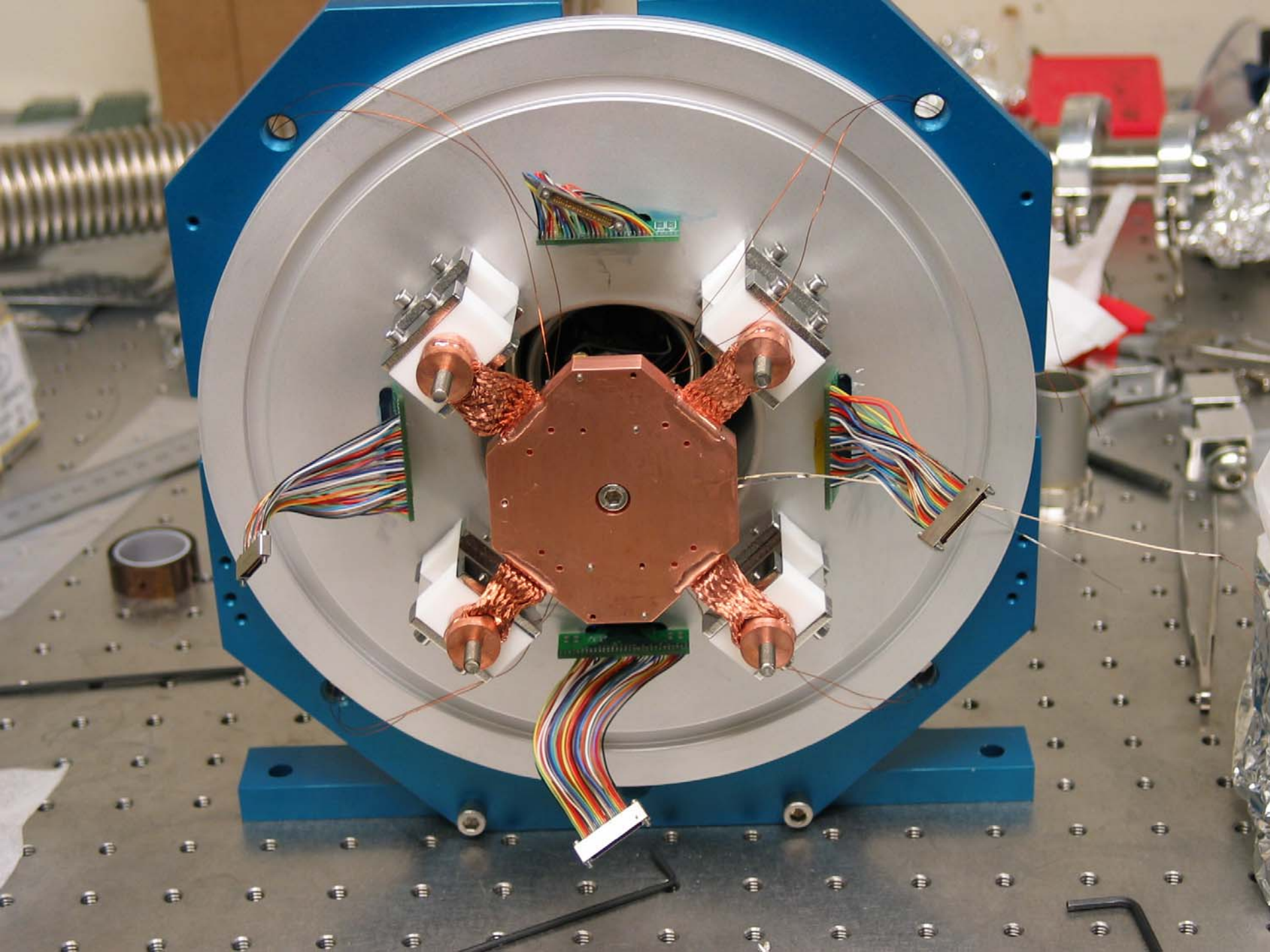
CCD_BOTTOM

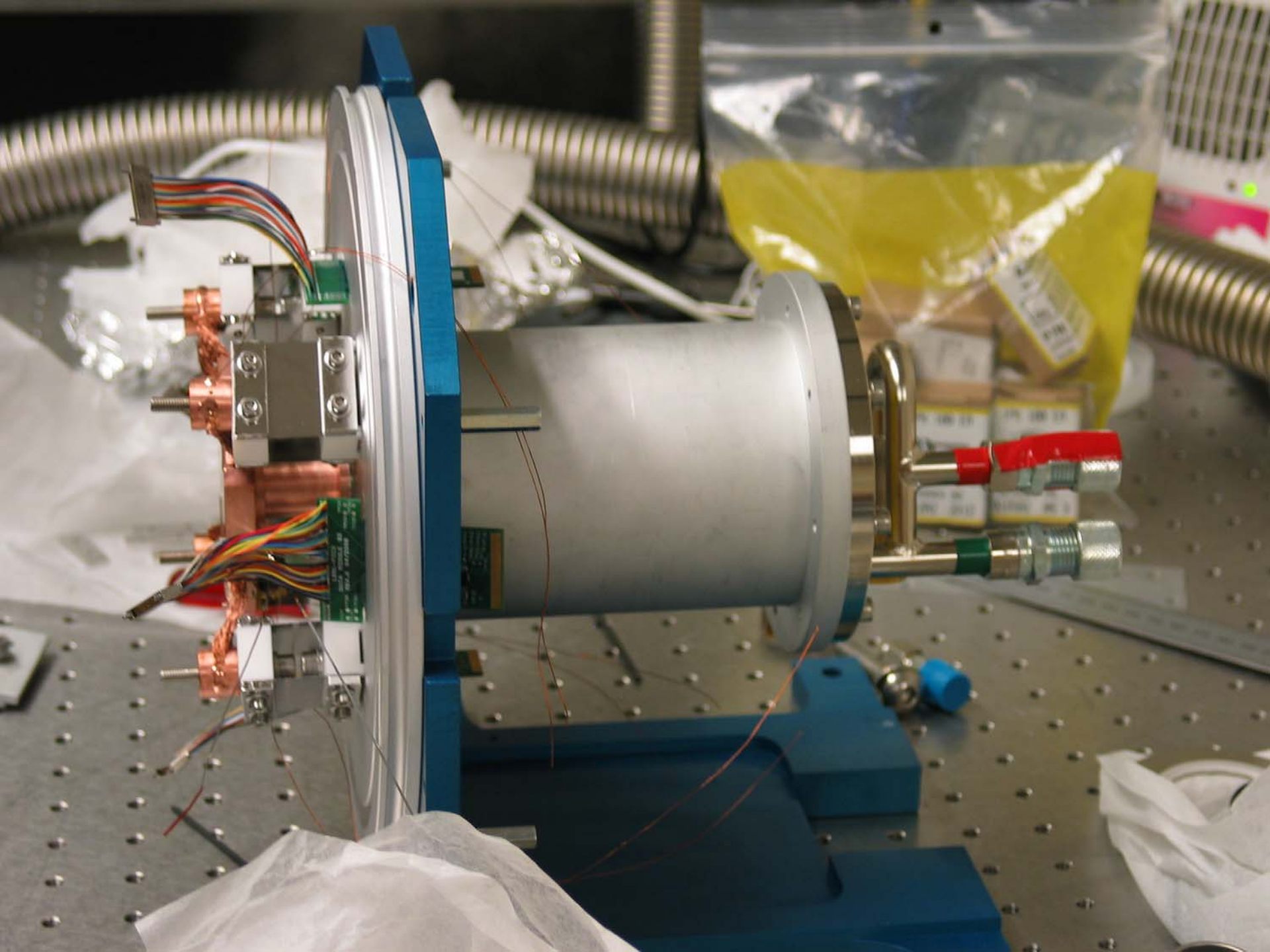
CCD_LEFT

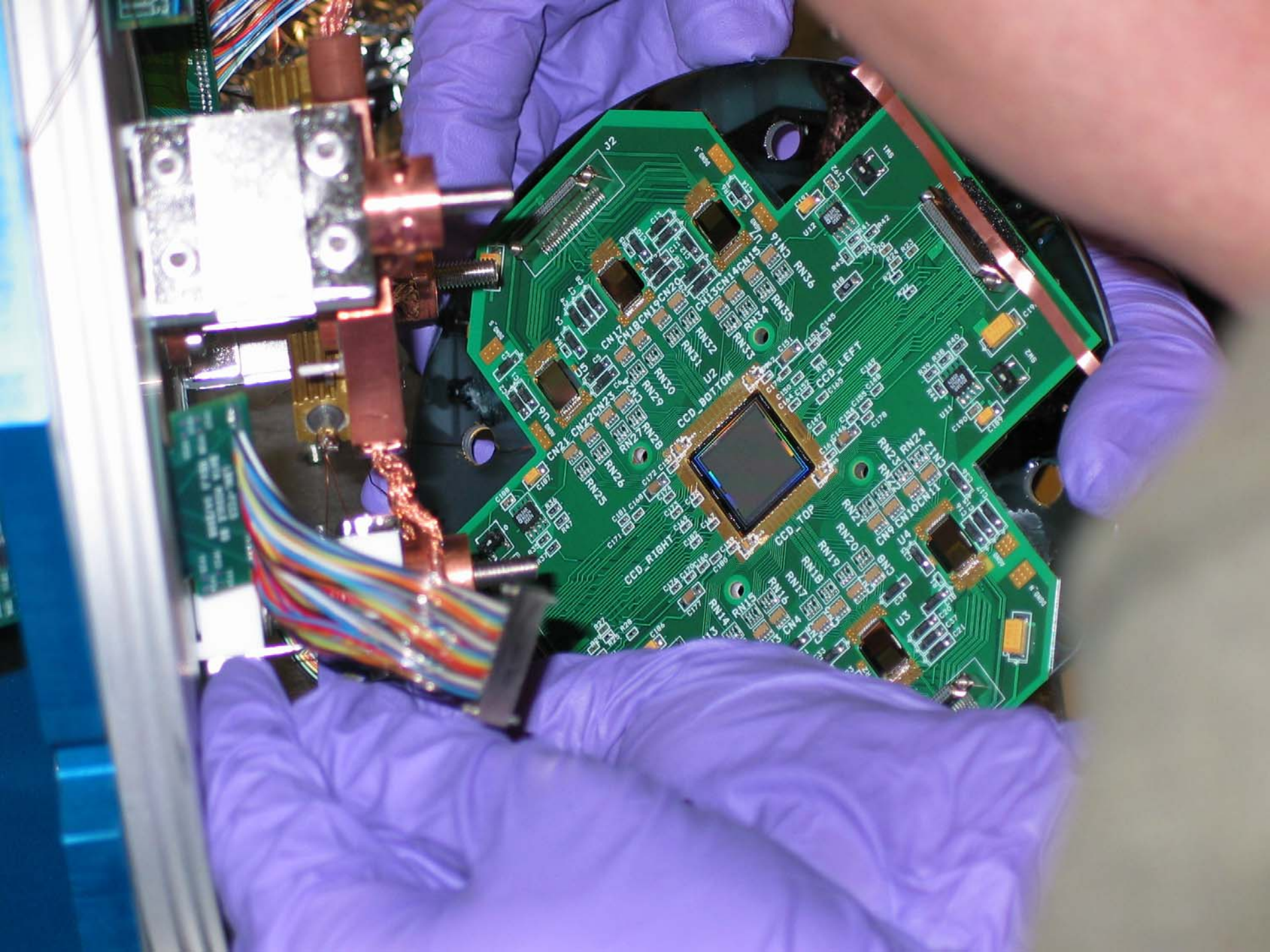
CCD_TOP

CCD_RIGHT

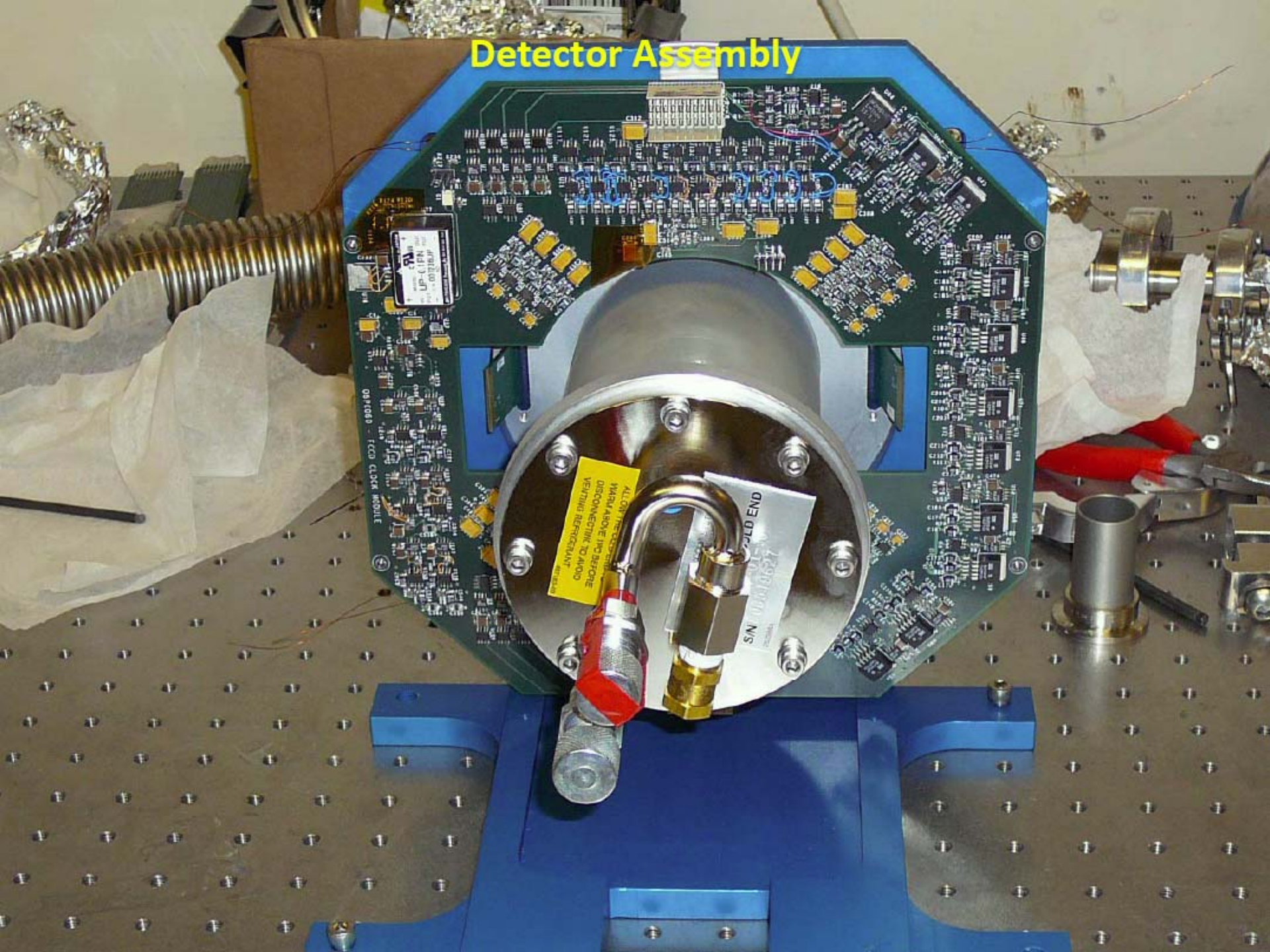








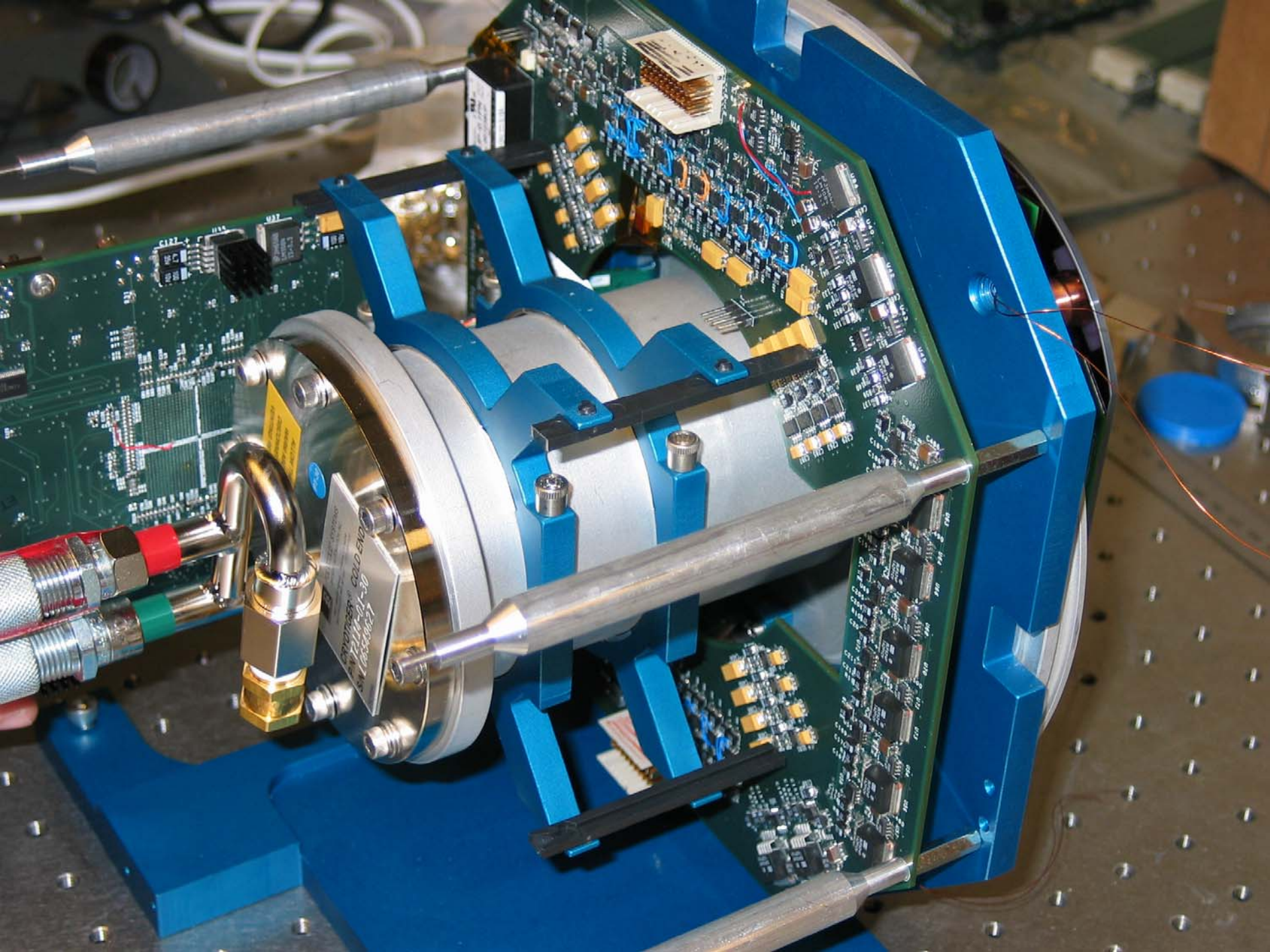
Detector Assembly



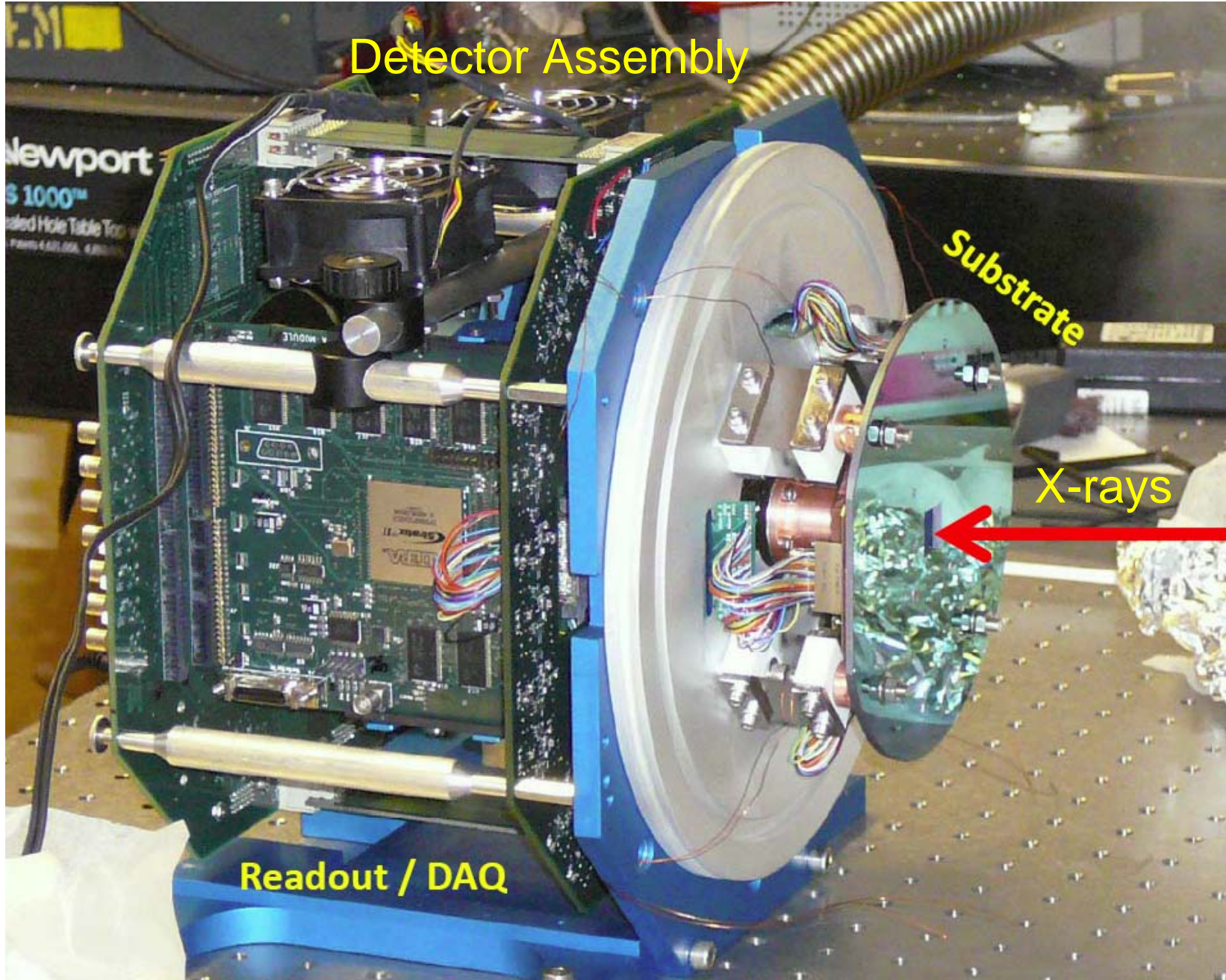
ALL ON THESE ENDS
HAND ASIDE THE BEFORE
DISCONNECTING TO AVOID
VENTILATION REFERENCE

OLD END
S/N: 00181812

081081 - FCCO CLASS MODULE



Detector Assembly



Substrate

X-rays

Readout / DAQ

APS/LBNL Collaboration on Fast CCD Detectors

■ Current Status

- Passed smoke test
- The camera is operating in a vacuum with cooling
- We can see visible light at 4 analog outputs and on some of the fCRIC digital outputs

■ Next Steps

- Finish Integration
- Characterize prototype detector
 - *Using visible light and x-rays*
- APS builds two sets of the final back end electronics
- LBNL builds two sets of final CCD assemblies and mechanical housings
- Targeting Fall for assembly of final system at APS

APS/LBNL Collaboration on Fast CCD Detectors

■ Acknowledgments

■ ANL

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- Tim Madden
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- Steve Ross
- Brian Tieman
- John Weizeorick

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- Matthew Church
- Dionisio Doering
- Peter Denes
- James Glossinger
- Alastair MacDowell
- Howard Padmore